Study on Three-phase Six-switch Buck-type Rectifier of High Power Factor

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Keywords: DSP28335, AC-DC power converters, Power factor correction, Energy efficiency.

Abstract. This paper proposed a three-phase six-switch buck-type APFC rectifier based on DSP28335. At present, the boost-type power factor correction rectifier has the advantages of high input current power factor and low harmonic distortion. However, it has the disadvantages of high EMI common-mode noise, and the high output voltage also produces negative effect to the DC-DC converter. This paper designed a three-phase six-switch buck-type APFC circuit, which has no shortcomings of the boost-type power factor correction rectifier, but retains the advantages of the boost-type rectifier, which has high input power factor, low harmonic distortion, low output voltage and low EMI common-mode noise. In addition, it has a high conversion efficiency. Finally a 117V input, 60V/138 watts output device is produced for verification.

Introduction

Rectifier plays a very important role in the converter device. At present, the input rectifier and filter circuit of many power electronic devices is composed of uncontrolled rectifier diode or capacitor filter circuit, so it will produce the problems such as low power factor and harmonic pollution. In power electronic equipment, a full-bridge rectifier is commonly used to convert 220V AC grid voltage to DC voltage. The input ac voltage is sinusoidal, but the input current is serious distorted which produced a large order of harmonic component[1].

In order to prevent input current harmonic pollution, many countries have different restrictions on the harmonics and power factor of the input current for rectifiers of different power ratings. The power supply for telecommunication equipment is usually a capacitance type input circuit, so the phase difference between its current and voltage will produce power loss. In order to meet the requirements of related regulations, the power factor correction circuit is required, as a result, the power factor and the input current quality are improved.

At present, power factor correction is usually achieved with a boost-type power factor correction rectifier. The boost type power factor correction rectifier has the advantages of high input current power factor and low harmonic distortion. But three-phase boost power factor correction in special applications, especially the application of charging pile has some disadvantages. For example, output voltage is too high and narrow range, so it is not conducive to the rear end design.

In this paper, a three-phase six-switch buck-type APFC circuit is designed. It has high input power factor, low harmonic distortion, low output voltage and low EMI common-mode noise. In addition, it has high energy efficiency. Finally, the correctness of the method is verified by experiments.

The Control Algorithm of Three-phase Six-switch Buck-type APFC

This design uses the three-phase six-switch buck-type APFC hardware block diagram as shown in Figure 1. This design using the topology designed to a stable DC output power factor correction rectifier, and guarantee the input current is sinusoidal wave and keep high efficiency.

First of all, the line voltages $U_{ab}$, $U_{bc}$ are collected by the voltage sensor Lv25-P, and then calculate the $U_{ca}$, and then calculate the $U_a$, $U_b$, $U_c$, finally using abc-dq transformation.
Phase-locked loop is used to obtain the phase-change voltage of each AD sampling period. A phase angle, $\theta_k+1=\theta_k+\omega T_s$, using phase-locked loop so that $\theta_k=0$, which is $\theta_{k+1}=\omega T_s$. Now, A phase voltage is $K\cos \theta_{k+1}$ ($K$ is a constant). A phase angle is $\theta_k+1$, B phase angle is $\theta_k+1-2/3\pi$, C phase angle is $\theta_k+1-4/3\pi$. The duty ratios $\delta_a$, $\delta_b$, and $\delta_c$ are calculated by the following equations:

$$
\begin{align*}
\delta_a &= M_x \cdot |\cos \theta_{k+1}|, \\
\delta_b &= M_x \cdot |\cos \theta_{k+1}-2/3\pi|, \\
\delta_c &= M_x \cdot |\cos \theta_{k+1}-4/3\pi|
\end{align*}
$$

where $M_x$ is a constant. However, this design has a high switching frequency, which has a very short sampling period, and in a period of relatively large amount of calculation. So in the actual program, the first list of the cosine value of the table, and then use the look-up table to be cosine, while the multiplication and division as far as possible with the shift or versus. Finally, the steady state error of the system is reduced by the PI regulator to improve the stability of the system.

In order to guarantee minimum switching loss as well as minimum input filter capacitor voltage ripple and minimum DC current ripple, the power period of the input voltage is divided into 12 equal areas, each of which is 30 degrees, as shown in Figure 2(a). The duty ratios $\delta_i$ of the PWM waves for each region is shown in the table 1[2,3]. DSP PWM wave is shown in Figure 2(b)(c)(d).

![Figure 1. Hardware block diagram.](image1)

![Table 1. Applied duty ratios by input voltage.](image2)

<table>
<thead>
<tr>
<th>Sector</th>
<th>Effective duty ratio $\delta_a$</th>
<th>Effective duty ratio $\delta_b$</th>
<th>Effective duty ratio $\delta_c$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$\delta_a$ 1- $\delta_c$+ $t_d$</td>
<td>$\delta_c$ 1- $\delta_a$+ $t_d$</td>
<td>$\delta_c$ 1- $\delta_a$+ $t_d$</td>
</tr>
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<td>2</td>
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<td>$\delta_b$ 1- $\delta_a$+ $t_d$</td>
<td>$\delta_b$ 1- $\delta_a$+ $t_d$</td>
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<tr>
<td>3</td>
<td>$\delta_a$ 1- $\delta_a$+ $t_d$</td>
<td>$\delta_a$ 1- $\delta_a$+ $t_d$</td>
<td>$\delta_a$ 1- $\delta_a$+ $t_d$</td>
</tr>
<tr>
<td>4</td>
<td>$\delta_c$ 1- $\delta_a$+ $t_d$</td>
<td>$\delta_c$ 1- $\delta_a$+ $t_d$</td>
<td>$\delta_c$ 1- $\delta_a$+ $t_d$</td>
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<tr>
<td>5</td>
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<td>$\delta_a$ 1- $\delta_a$+ $t_d$</td>
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<tr>
<td>7</td>
<td>$\delta_b$ 1- $\delta_a$+ $t_d$</td>
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<tr>
<td>9</td>
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<tr>
<td>12</td>
<td>$\delta_a$ 1- $\delta_a$+ $t_d$</td>
<td>$\delta_a$ 1- $\delta_a$+ $t_d$</td>
<td>$\delta_a$ 1- $\delta_a$+ $t_d$</td>
</tr>
</tbody>
</table>

Where $t_d=1\mu S$

![Figure 2. DSP PWM waveform.](image3)
The Hardware Implementation

The Main Circuit
This design uses the three-phase six-switch buck-type APFC hardware block diagram as shown in Figure 1. The design of the output inductor is divided into L1 and L2, and L1 = L2 in order to provide symmetric attenuation impedances for conducted common-mode noise currents.

Sampling Circuit
The design of voltage sampling to use voltage sensor Lv25-P to the voltage amplifier and filter circuit of Figure 3(a), passed to DSP28335 and let DSP analysis and processing. Protection of voltage acquisition circuit is shown in Figure 3(d). If VDCCOM1 voltage more than 10V, the output voltage of the VDCP_IN from positive voltage will jump to negative voltage. When the voltage jumped, the system will stop working, so it have effect of over voltage protection.

When using DSP28335 ADC conversion module, the A/D of DSP28335 input voltage range is 0-3V. If input negative voltage or positive voltage higher than 3V, it will damage the A/D module. But the input voltage is sinusoidal AC voltage, it can't use the circuit of Figure 3(a), and need voltage processing of trailing end, as shown in Figure 3(b). It adds a conversion circuit based on Figure 3(a), which solved the problem that input negative voltage damages A/D module. This design has two input voltage acquisition module, which used to collect V_ab and V_bc respectively, and then calculated the value of U_a and U_b.

The design of current sampling to use current sensor La100-P to the current amplifier and filter circuit of Figure 3(c), passed to DSP28335 and let DSP analysis and processing. Similarly, the input current is sinusoidal AC current, so the trailing end is also needed a conversion circuit.

The Power Supply Module
The design of the control circuit power supply is shown in Figure 4(a). Input 24V DC voltage passes the DC/DC converter TEN5-2411, and then output 5V DC voltage.

The design of IGBT drive power supply is shown in Figure 4(b). Input 24V DC voltage passes the DC/DC converter TEN20-2413, and then output 15V DC voltage.

The design of the analog signal processing power circuit is shown in Figure 4(c). Input 24V DC voltage passes the DC/DC converter TEN20-2423, and then output ±15V DC voltage.

The design of the power conversion circuit is shown in Figure 4(d). Input 24V DC voltage passes the REF5030 DC/DC converter, and then output 3V DC voltage.

The design of DSP28335 power is shown in Figure 4(e). Input 24V DC voltage passes the LM2596-3.3 DC/DC converter, and then output 3.3V DC voltage.
IGBT Driver

This design uses the three-state output 16-bit 2.5V to 3.3V / 3.3V to 5V level translator SN74LV164245 to turn DSP28335 output 3.3V PWM wave (for example PWM1A) to 5V PWM wave (for example HPWM1A), as shown in Figure 5(a).

![Control circuit power supply circuit](image1)

![IGBT drive power supply circuit](image2)

![Analog signal processing power supply circuit](image3)

Figure 4. Power supply circuit.

HPWM wave first passes high-speed MOSFET drive UCC27423DR with enable pin, and then passes IGBT driving optocoupler HCPL–3120. Finally, it can make signals of IGBT driving, as shown in Figure 5(b). IGBT’s error signal SO_A passes optocoupler TLP121 to IGBT_PA_IN.

![Voltage transformation](image4)

![IGBT drive optocoupler](image5)

Figure 5. IGBT Driver.

Experimental Verification

The design of the experimental parameters are as follows: Po=138W, Ui_rms=117V, Io=2.3A, M=0.24, fp=12.8kHz, Lo=2mH, Li=0.7mH, Ci=1uF, Ro=26Ω.

Where Po is the output power, Ui, rms the input voltage RMS, Io the output voltage, M the modulation index, fp the IGBT switching frequency, Lo the output inductor, Li the input inductance, Ci input capacitance and Ro the output resistance.

The experimental results are shown in Figure 6. The green curve above in Figure 6 is the values of A phase current, and the black curve below in Figure 6 is the values of A phase voltage. The red line below in Figure 6 is the output DC voltage. By the experimental results, it can be seen that the output DC voltage is basically a straight line, there is almost no ripple. The grid current passes the
power factor correction, finally it is almost completely consistent with voltage phase. The product picture is shown in Figure 7.

![Figure 6. The input voltage current and output voltage waveform.](image)

![Figure 7. Product picture.](image)

**Summary**

In this paper, a three-phase six-switch buck-type APFC circuit is designed, which has no shortcomings of the boost-type power factor correction rectifier, but retains the advantages of the boost-type rectifier, which has high input power factor, low harmonic distortion, low output voltage and low EMI common-mode noise. In addition, it has a high energy efficiency. The experimental results also prove the correctness of this design method.

**Acknowledgement**

This work is financially supported by the National Science Foundation for Young Scientists of China (Grant No. 51407131)

**References**

