Research on LCD-VGA Conversion Technology Based on ARM Microprocessor

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ABSTRACT

LVDS-VGA conversion design for embedded system is proposed by using VGA interface timing as standard, ARM chip S59V210 as CPU, and D/A chip SDA7123 for signal conversion. On one hand, LCD controller of S5PV210 chip is configured to allow digital signals to be generated via LVDS interface. On the other hand, D/A chip SDA7123 converts digital signals into analog signals, enabling normal video displaying on VGA interface terminal. This solution has been proven to deliver good display results for video signals of varying resolution, like 800*600, 1024*768. It features low system impact, high efficiency and reliability, suitable to be widely adopted in embedded application.

INTRODUCTION

LCD controller is integrated in many embedded microprocessors, e.g. S5PV210 and S3C6410 of Samsung, ATSAMA5D3 series processors of Atmel. It enables convenient connection to large LCD displays, which, however, are very expensive. In comparison, LCD displays for PC are commonly seen. If they can be utilized as display terminal, a number of advantages are available: reasonable use of existing resource, saving system cost, little space occupied, and easy to carry. VGA interface is a standard for inputting signal into LCD display of most PCs. LVDS-VGA signal conversion is proposed to solve this problem. After analyzing the relation between VGA display timing and LCD display timing, a key point is found, and the feasibility is verified.

VGA INTERFACE

Video Graphics Array, VGA, is a display standard using analog signals, and it was proposed by IBM in 1987. VGA interface has 15 pins in 3 rows, with 5 poles for each row, as displayed in Fig. 1.

![VGA Interface](image1.png)

**Figure 1.** VGA Interface.
VGA interface uses analog signals, mainly red, green, blue, as well as horizontal sync, and vertical sync. Pin definitions are shown in Table 1.

**Table 1. Definitions of VGA Pins.**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Description</th>
<th>Pin</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RED</td>
<td>red component signal</td>
<td>9</td>
<td>+5V</td>
<td>5V voltage</td>
</tr>
<tr>
<td>2</td>
<td>GREEN</td>
<td>green component signal</td>
<td>10</td>
<td>SGND</td>
<td>ground</td>
</tr>
<tr>
<td>3</td>
<td>BLUE</td>
<td>blue component signal</td>
<td>11</td>
<td>NC</td>
<td>unused</td>
</tr>
<tr>
<td>4</td>
<td>NC</td>
<td>unused</td>
<td>12</td>
<td>DDC DATA</td>
<td>DDC data signal</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>ground</td>
<td>13</td>
<td>HSYNC</td>
<td>Horizontal sync</td>
</tr>
<tr>
<td>6</td>
<td>RGND</td>
<td>red component ground</td>
<td>14</td>
<td>VSYNC</td>
<td>Vertical sync</td>
</tr>
<tr>
<td>7</td>
<td>GGND</td>
<td>green component ground</td>
<td>15</td>
<td>DDC_CLK</td>
<td>DDC clock signal</td>
</tr>
<tr>
<td>8</td>
<td>BGND</td>
<td>blue component ground</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**ANALYSIS OF VGA TIMING AND LCD TIMING**

VGA timing divides into horizontal timing and vertical timing. Horizontal timing is shown in Fig. 2:

It mainly includes horizontal line width, back porch (HBPD+1), front porch (HFPD+1), sync (HSPW+1), and display interval (HOZVAL+1).

Horizontal line width = (HBVD+1) + (HFPD+1) + (HSPW+1) + (HOZVAL+1)

Each part functions as follows:

1) HBPD: Used to confirm the blanking interval before horizontal sync signal and horizontal data transmission, and to describe the amount of VCLK pulses within the delay before data transmission

2) HFPD: Used to confirm the blanking interval between the completion of data transmission and the coming of next horizontal sync signal, and to describe the amount of VCLK pulses within the delay after data transmission

3) HSPW: Used to confirm the horizontal sync clock pulse width, and to describe the amount of VCLK pulses within the horizontal sync pulse width

4) HOZVAL: Used to confirm the horizontal display size

Vertical timing is shown in Fig. 3:
It mainly includes vertical line width, back porch (VBPD+1), front porch (VFPD+1), sync (VSPW+1) and display interval (LINEVAL+1).

Vertical Line Width = (VBVD+1) + (VFPD+1) + (VSPW+1) + (LINEVAL+1)

Each part functions as follows:

1) VBPD: Used to confirm the blanking interval before frame sync signal and frame data transmission, and is the ratio of delay time before frame data transmission to the width of the line sync clock interval

2) VFPD: Used to confirm the blanking interval between completion of frame data transmission and the coming of next frame sync signal, and is the ratio of delay time after frame data transmission to the width of the line sync clock interval

3) VSPW: Used to confirm the width of frame sync clock pulse, and is the ratio of the width of frame sync signal clock to the width of the line sync clock interval

4) LINEVAL: Used to confirm the vertical display size

A typical LCD timing diagram is as shown in Fig. 4. Compared with VGA timing, LCD scanning timing is similar to VGA timing, which makes possible for LCD controller to generate timing signals required by VGA, and offers theoretical basis for LVDS to VGA conversion.
To make this possible, the following questions should be solved:

1) Since sync signals of VGA interface are active high, while sync signals of S59V210 LCD interface are active low, level converting must be solved;
2) Red, green, and blue channels of VGA interface are of analog quantity, but S5PV210 LCD controller outputs RGB digital signal. This means D/A conversion must be adopted to turn digital signals into analog signals, thus enabling signal matching.

DS90CF364A chip and D/A chip SDA7123 are used for signal conversion.

INTRODUCTION TO DS90CF364A AND SDA7123 CHIPS

DS90CF364A receiver can convert 4-channel LVDS data stream into parallel 28-bit CMOS/TTL data (24-bit for RGB and 4-bit for Hsync, Vsync, DE and CNTL). Besides, DS90CF364A can also convert 3-channel LVDS data stream into parallel 21-bit CMOS/TTL data (18-bit for RGB and 3-bit for Hsync, Vsync, and DE). Output of both receivers uses falling edge gate. Interoperability is possible between a rising edge or falling edge gate sender (DS90C383A/DS90C363A) and a falling edge gate receiver even if there is no transmission logic.

Compared to its predecessor, DS90CF364A features offer a wider data valid time in output, and Fig. 5 shows its structure diagram:

SDA7123 is a 3-channel 10-bit video D/A converter that can convert R (red), G (green) and B (blue) signals. It belongs to current output, and the green channel can output sync signals. Its data update frequency MSPS is 140MHZ, and reference voltage is at 1.23V, and working temperature of -40~+85oC. It is applicable to digital video system, image processing, instrument, high-precision display, and video signal reconstruction, and can be replaced by ADV7123.

Its schematic diagram is as shown in Fig. 6:

SDA7123 has three independent 10-bit input interfaces, and can work with single power of 5V or 3.3V. In addition, SDA7123 has two supplementary video control signals: composite (sync signal) and (black level).
CIRCUIT DESIGN FOR LVDS-VGA INTERFACE

To enable LVDS-VGA conversion, the interface circuit is designed as follows:
1) Use DS90CF364A chip for converting 3-channel LVDS data stream to parallel 21-bit CMOS/TTL data
2) The 21-bit CMOS/TTL data generated by DS90CF364A chip includes 18 bits for RGB data, which will be input into SDA7123, enabling the D/A conversion from LVDS to VGA.

The schematic diagram is shown in Fig. 7:

Figures 6 and 7 show the schematic diagrams for the LVDS-VGA interface and the circuit design, respectively.

SETTING OF LCD CONTROL REGISTER OF S5PV210 CHIP

VGA output supports a number of resolution display modes, which have different timing parameters. Therefore, an output resolution should be selected firstly. Then, the LCD controllers should be configured to generate corresponding timing parameters. PC display is used as display output end in this plan, and PC displays of most manufacturers support VESA standard. With that considered, this standard is used for setting LCD controller parameters, which would guarantee that VGA output generated can be displayed normally on PC displays of most brand manufacturers.
Because VGA display output of 800*600 resolution and 60HZ refresh rate could not be properly supported in some brand PC displays, 16-bit colorful VGA display of 1024*768 resolution and 75HZ refresh rate is selected for detailed analysis of LCD control register setting. The VESA standard offers value ranges for horizontal timing and vertical timing for VGA display at 1024*768 resolution and 75Hz refresh rate, as shown in the Table 2 below:

<table>
<thead>
<tr>
<th>Name</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hor Sync Time</td>
<td>1.219us</td>
</tr>
<tr>
<td>H Back Porch</td>
<td>2.235us</td>
</tr>
<tr>
<td>H Front Porch</td>
<td>0.203us</td>
</tr>
<tr>
<td>Hor Addr Time</td>
<td>13.003us</td>
</tr>
<tr>
<td>Hor Total Time</td>
<td>16.660us</td>
</tr>
<tr>
<td>Ver Sync Time</td>
<td>0.05ms</td>
</tr>
<tr>
<td>V Back Porch</td>
<td>0.466ms</td>
</tr>
<tr>
<td>V Front Porch</td>
<td>0.017ms</td>
</tr>
<tr>
<td>Ver Addr Time</td>
<td>12.795ms</td>
</tr>
<tr>
<td>Ver Total Time</td>
<td>13.328ms</td>
</tr>
</tbody>
</table>

Value ranges in Table 2 are used for setting LCD control registers. First of all, it should be stated that Src_clk (Frequency of Clock source) value is 166750000Hz in this case, which is a base for setting the values of the following control registers.

1) VIDCON0 register

CLKVAL_F: To confirm the ratio of VCLK to CLKVAL[7:0]. When CLKVAL >=1, VCLK=HCLK/(CLKVAL+1).

In this case, HCLK=166.75MHz, VCLK=Pixel Clock=78.75MHz, so CLKVAL should be set as 1.

L1_DATA16: secondary i80 interface (LDI1) data output format and 16bpp mode are selected in this design, then set L1_DATA16=000.

L0_DATA16: secondary i80 interface (LDI0) data output format and 16bpp mode are selected in this design, then set L0_DATA16=000.

2) VIDTCON0 register

VBPD: According to data in Table 2, VBPD=(V Back Porch)/(Hor Total Time)=0.466ms/16.660us≈28

VFPD: According to data in Table 2, VFPD=(V Front Porch)/(Hor Total Time)=0.017ms/16.660us≈1

VSPW: According to data in Table 2, VSPW=(Ver Sync Time)/(Hor Total Time)=0.05ms/16.660us≈3

3) VIDTCON1 register

HBPD: Because VCLK=Pixel Clock=78.75MHz=12.6984ns, and according to data in Table 2, HBPD=(H Back Porch)/(Pixel Clock)=2.235us/12.6984ns=176

HFPD: Same as above, HFPD=(H Front Porch)/(Pixel Clock)=0.203us/12.6984ns≈16

HSPW: Same as above, HSPW=(Hor Sync Time)/(Pixel Clock)=1.219us/12.6984ns≈96

4) VIDTCON2 register

LINEVAL: Because a resolution of 1024*768 is used, then LINEVAL=(Horizontal display size)-1=1023

HOZVAL: HOZVAL=(Vertical display size)-1=767

5) WINCON0 register
BPPMODE_F: A display mode of 16bpp(R:5-G:6-B:5) is used, then BPPMODE=5

The above setting can guarantee signal conversion from LVDS to VGA. Since passthrough is adopted for hardware circuit, as long as registers for LCD controllers are set properly, video or image information can be output to VGA display via SDA7123 D/A conversion.

TESTING

When S5PV210 LVDS interface is connected to VGA interface via the hardware circuit of this plan, and corresponding LCD control registers are properly configured, normal video or image output can be achieved. Display results are shown in Fig. 8:

![Figure 8. Display Results.](image)

CONCLUSION

This paper proposes a method to enable VGA display by using S5PV210 LCD controller. By analyzing LCD interface timing and VGA interface timing for similarities, this paper proves the feasibility of LVDS-VGA conversion interface. LCD control register is configured to generate LVDS digital signals, which are then converted into TTL signals via DS90CF364A chip, and last into analog signals that VGA interface needs via D/A chip SDA7123. Results show that LVDS-VGA conversion circuit can display the image well on screen with VGA interface, and can meet the demand of numerous common users. This solution features low cost and easy operation, and is suitable to be widely adopted for engineering concerned.
REFERENCES