Large Storage Window in a-SiNx/nc-Si/a-SiNx Sandwiched Structure

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ABSTRACT

The a-SiNx/nc-Si/a-SiNx sandwiched structures have been fabricated by plasma enhanced chemical vapor deposition (PECVD) technique at low temperature (250°C). Si nanocrystal (nc-Si) layer is fabricated from a hydrogen-diluted silane gas mixture with a layer-by-layer technique in a PECVD reactor. Atom force microscopy measurement shows that the density of nc-Si is about 2×10¹¹ cm⁻². The charging and discharging of nc-Si quantum dots is studied by capacitance-voltage (C-V) measurement at room temperature. An ultralarge hysteresis which is attributed to injecting the electrons and holes into the nc-Si dots is observed in the C-V characteristic. The largest shift of the flatband voltage (ΔV_FB) of the sample is above 8 V. The number of electron stored in each nc-Si quantum dot estimated from the ΔV_FB is close to 8. A model is put forward to interpret the ultralarge hysteresis phenomena and mechanism of the charge storage in detail.

INTRODUCTION

Currently, the MIS structure containing silicon quantum dots has attracted great interest both for new physical phenomena and for potential application in future single electron transistors, switching devices and memory devices [1-6]. Several research groups have investigated charge storage effects in silicon nanostructures and reported on their potential applications to memory devices [7,8]. The flash-memory devices based on silicon quantum dots have characteristics that include long-term charge storage, fast response, and low power requirement. However, these devices are sensitive to the surface states because only a small number of electrons are used in the memory operations. Recently, several MIS structures have been carefully fabricated to ensure a negligible concentration of interface traps so that the measured Capacitance-voltage (C-V) characteristic is due predominantly to effect of the nanocrystal [9].

In this paper, we report the fabrication of a-SiNx/nc-Si/a-SiNx sandwiched structure on the silicon substrate by plasma enhanced chemical vapor deposition (PECVD) technique at low temperature (250°C). From the C-V and

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Conductance-voltage (G-V) characteristic, an ultralarge hysteresis is observed which means a large number of charges are stored in the sample. The dependence of frequency of C-V measurements show that there are no capacitance shoulders and distortions around the flatband voltage in the C-V curves, which means the interface defect states is negligible. A model is forward to interpret the ultralarge hysteresis phenomena.

EXPERIMENT DETAILS

The sandwiched structures (a-SiN$_x$/nc-Si/a-SiN$_x$) were deposited on a substrate of n-type (100) crystalline silicon (6–8 Ω/cm) in a PECVD system at 250 °C with an rf power of 50 W. First, a thin tunneling SiN$_x$ layer of 2 nm was deposited by a gas mixture of silane and ammonia. Then, an nc-Si array layer was fabricated from a hydrogen-diluted silane gas mixture with a layer-by-layer technique. Finally, a thick gate SiN$_x$ layer was deposited following the same conditions as those of the tunneling SiN$_x$ layer. After that the sample was annealed in N$_2$ ambient at 900°C for 30 minutes to improve the quality of the nc-Si and reduce the interface state and defects in the structure. Al electrodes with an area of 1×10$^{-3}$ cm$^2$ on the topside and backside were made with the vacuum evaporation method.

The C-V characteristics were measured at room temperature using an Agilent 4284A precision LCR meter. All measurements were performed at air ambient and at room temperature inside a shield box.

Atom force microscopy (AFM) was used to characterize the size and distribution of the nc-Si array in the sample. In order to the AFM measurement, a designed sample was made following the same programming except for without the thick gate SiN$_x$ layer. The plane-view AFM image of the designed sample shows that the shape of nc-Si dots is roughly spherical and the mean size is 5 nm with a deviate of less than 10%. The density of nc-Si is estimated to be 2×10$^{11}$ cm$^{-2}$.

RESULTS AND DISCUSSION

The typical C-V and G-V characteristics shown in Fig. 1 are obtained by sweeping the voltage between inversion and accumulation regions at room temperature. The sample is first held at a gate voltage of -1V for 60 s in order to allow saturation positive charge storage, followed by a gate voltage sweep from -1 V to 1 V. At the end of this forward sweep, the sample is held at a gate voltage of 1 V for 60 s to allow saturation negative charge storage and then followed by a reverse sweep from 1 V to -1 V. The voltage sweep range is then increased from -1 V<V$_g$<1 V to -9 V<V$_g$<9 V in steps of 0.5 V.
A big clockwise hysteresis is observed in both C-V and G-V characteristics, which is caused by the successive charge trapping and de-trapping processes in nc-Si. From the C-V plot, the flatband voltage $V_{FB}$ is determined for each C-V curve from the flatband capacitance value of $4.0 \times 10^{-11}$ F. Fig. 2 demonstrates the gate voltage dependence of flatband voltage. As can be seen here, a higher gate voltage results in a wider corresponding hysteresis, which means more and more charges are stored in the nc-Si and at a gate voltage of above 7 V, the hysteresis width changes hardly, which means the saturation charge storage. Here the total hysteresis width is the sum of the flatband voltage shifts due to electron and hole charging. The due to the electron and hole charging is 4.6 V and 3.5 V, respectively. We also measured the frequency dependence of C-V characteristic. We find the magnitude of the capacitance hysteresis almost remain unchanged at different frequency. As the interface state related strongly to the frequency, the hysteresis maybe results mainly from the charge that is trapped in the discrete energy levels of the nc-Si, and not from the interface state between nc-Si and the environmental. The total of charge is estimated from the shift of $V_{FB}$, $Q = \Delta C \cdot \Delta V_{FB} = 2.3 \times 10^{-10}$ C. From the AFM
results, the density of nc-Si is $2 \times 10^{11}$ cm$^{-2}$, hence the numbers of electron trapped in every nc-Si can be estimated to 7, which means there are at least seven discrete levels are taken up by electron. In order to interpret the phenomena, the energy level inside the nc-Si must be calculated. Two effects are playing a role in energy state, one is the quantum confinement effect and the other is the coulomb blockade effect. The quantum confinement effect provides discrete levels, and the coulomb blockade effect implies energy spacing between carriers in those confinement levels. The coulomb blockade energy is estimated according to a semiclassical constant-interaction (CI) theory. For nc-Sis (average diameter of 5 nm) floating above the silicon substrate, the capacitance of individual dot is estimate to be

$$C_{QD} = 4 \pi \varepsilon_0 \varepsilon_{SiN} R = 2.2 \times 10^{-18} F$$

(1)

with $R=2.5$ nm as radius of the nc-Si. The corresponding coulomb blockade energy is

$$E_{CB} = \frac{q^2}{C_{QD}} = 72 \text{meV}$$

(2)

with $q$ as the elementary charge. For quantum confinement, an infinite spherical square well model is employed to approximately estimate the energy levels of nc-Si as follow

$$E_n = \frac{\hbar^2}{2m_{Si}} \zeta_{n,0}^2$$

(3)

with $m_{Si}=0.26 m_0$, where $m_0$ is the rest electron mass, and is the nth zero point of the spherical Bessel function $j_l(r)$. From this formula, the first three energy levels are calculated to be 0.232 eV, 0.927 eV, and 2.085 eV, respectively.

![Figure 3. The schematic band diagrams of the sample.](image)

Taking an energy barrier between Si and SiN$_x$ of 1.5 eV, the second excited state is already delocalized. Only the ground state and first excited state are confined in the well. Because of the spin degeneracy, there are two ground state levels and six first excited state levels in the well, which is consistent with the result from our experiments. Being based on above discuss, a schematic band diagram of the sample is shown in the Fig. 3. As is shown in the diagram, when a positive voltage is applied to the gate, the Fermi level of the n-type silicon moves upward. When the Fermi level
is aligned to the discrete level of the nc-Si, the electron can tunnel into nc-Si and be trapped. With increasing the gate voltage to 7 V, the Fermi level of n-type silicon is higher than all the discrete level in the well, hence all the levels are taken up by electron and no more electrons can tunnel into nc-Si dots.

SUMMARY

We have successfully fabricated a-SiNₓ/nc-Si/a-SiNₓ sandwiched structure on n-type silicon substrate by layer-by-layer deposition technique at low temperature in a PECVD reactor. AFM photography indicates that the nc-Si dots have a good size uniform and the dot density is $2 \times 10^{11}$ cm$^{-2}$. By capacitance measurement, we study the charging effect of the structure and an ultralarge hysteresis, whose width is above 8 V, is observed in the C-V characteristic. We find that there are no shoulders and distortions near the flatband voltage and the magnitude of the hysteresis is almost independent of frequency. Hence, the discrete quantum energy levels, rather than the interface state, are the primary cause of charge trapping and storage. The number of electron stored in each nc-Si quantum dot estimated from the $\Delta V_{FB}$ is close to 7. We also calculate the confinement energy level inside the nc-Si and there are 8 discrete levels inside the nc-Si dots. The values are close and saturation model could interpret the ultralarge hysteresis phenomena in our a-SiNₓ/nc-Si/a-SiNₓ sandwiched structures.

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