Implementation of the High-resolution Image Compression Algorithm based on 89s52S Single Chip Microcomputer

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Abstract

This paper conducts the analysis on the high-resolution image compression (IC) algorithm based on 89s52S single chip microcomputer. Image compression is an important issue in the field of image processing, at present, most algorithms, such as JPEG algorithm that compress all regions of the image with the same compression ratio. However, this kind of compression algorithm has its own inherent flaws, such as the gray discontinuity (block effect) at the boundary of each block, which will greatly affect the subjective quality of the reconstructed image. Under this basis, this paper proposes the novel IC algorithm and applies it on the hardware. The result proves the effectiveness.

Keywords: High-resolution, Image Compression, Algorithm, Single Chip Microcomputer

Introduction

The fractal image compression process mainly is approaches the source image using the compression mapping fixed point to complete the image the code, the image reconstruction is realizes through the iteration, this kind establishes above the fractal rationale the image compression method has the very great compression ratio has the widespread application prospect in image compression processing. When the image is complex or the precision of compression is high, it is difficult to obtain satisfactory results through one-time coding. In this paper, we propose a class of the fractal image compression method based on the pre-processing-correction mode. If the quality of the compressed image is not satisfactory, we retain the existing results as a pretreatment, and then propose a correction method to improve the pre-processing results. In this way, double counting can be avoided. Because of the use of the existing calculation results, the coding process of the correction process becomes relatively easy, which is a kind of fractal image compression method which is easy to be applied in practice.

Figure 1. The Demonstration of the High-resolution Image Compression.
As demonstrated in the figure one, we show the high-resolution image compression model, in the following sections, we will propose our new methodologies on this challenge.

The Proposed Methodology

High-resolution Image Compression Algorithm. The hyperspectral image has the high spectral resolution, but the spatial resolution is low and the mixed pixels are common, which brings great difficulties to the corresponding application. Hardware is mainly by reducing the size of the basic photosensitive components, increase the pixel density and sampling frequency, but because of the high cost while making this approach difficult to achieve. Image compression is an important issue in the field of image processing, at present, most algorithms, such as JPEG algorithm that compress all regions of the image with the same compression ratio. However, this kind of compression algorithm has its own inherent flaws, such as the gray discontinuity (block effect) at the boundary of each block, which will greatly affect the subjective quality of the reconstructed image. At the same time, size of the block, by discarding some of the high-frequency coefficient to obtain the compression effect, so only a low degree of the general compression ratio.

\[
\begin{bmatrix}
Y \\
Cb \\
Cr
\end{bmatrix} = \begin{bmatrix}
0.299 & 0.587 & 0.114 \\
-0.169 & -0.334 & 0.500 \\
0.500 & -0.419 & -0.081
\end{bmatrix} \begin{bmatrix}
R \\
G \\
B
\end{bmatrix} + \begin{bmatrix}
0 \\
128 \\
128
\end{bmatrix}
\]

(1)

As shown in the formula one, we define the image transformation function, with the general core reference that as a result of the PCNN connection territory characteristic, causes when some neuron internal active item is bigger than the dynamic threshold value to output pulse 1, around this neuron in the neighborhood has the approximate input drive other neurons when the next time iteration, is connected the input the influence also to activate the output pulse. Therefore has the approximate gradation picture element correspondence neuron to connect the territory the characteristic which but the function the synchronization activates to cause PCNN to be extremely suitable takes the division image coding the division algorithm which can be reflected as the equation 2.

\[
A = \frac{\sum_{K=0}^{K-1} s_{j}(k) \left( -x_{k}^{2} + x_{K-1}x_{k} \right)}{\sum_{K=0}^{K-1} \left( -x_{k}^{2} + x_{K-1}x_{k} \right)^{2}}
\]

(2)

Where the \( \sum_{K=0}^{K-1} \left( -x_{k}^{2} + x_{K-1}x_{k} \right)^{2} \) represents the basis function, the PCNN in iteration of the output value of two images according to spatial adjacent or not marked different regions, the same operation on each iteration, until all pixels corresponding neurons are activated once. Thus, the pixels in each segmentation region have gray value and spatial approximation simultaneously. Our model can be then described as the follows. The multi-scale Wedgelet analysis can be divided into multi-scale Wedgelet decomposition and multi-scale Wedgelet representation. The MWD divides the image into scale image blocks and projects each image block into the permissible azimuthal Wedgelet MWR using the MWD results. (1) According to the quadtree structure from the ground from the top to the bottom of the original image of the depth of the original image of the MWD; (2) According to the quad-tree structure from the
ground; (3) According to the general quadratic tree decomposition structure of the encoded image MWR coefficients, so as to code the edge of the image contours. And the evaluation functions can be defined as formula 3 and 4.

\[
MSE = \sqrt{\frac{1}{WH} \sum_{x=0}^{W-1} \sum_{y=0}^{H-1} [f(x, y) - f'(x, y)]^2}
\]

(3)

\[
PSNR = 20 \log_{10} \frac{255}{MSE}
\]

(4)

As the initial primary function, in has carried on in the division foundation to the image, carries on the standard orthogonalization to each division region, obtains corresponds each division region the group of standard orthogonal primary function, and thus obtains should divide the region image the approximate function and the compressed image is compressed with high compression ratio (the significance of different regions is different in the background, the background region with the low significance can be compressed with higher compression ratio), and the compressed image has ROI information which can be demonstrated as the figure 2.

![Figure 2. The Paradigm of the Proposed Compression Algorithm.](image)

**The Image Processing Hardware Implementation.** In order to achieve static image processing, we need to meet the following conditions: First, in order to real-time image processing, processor speed has certain requirements; Secondly, the image processing of large amount of data, therefore, DSP chip memory chip to meet certain size. Considering all the above factors, we consider TMS320VC5509A of TI, HY57V641620 of DARAM, AM29LV800 of FLASH, and MAX II of the Altera as the interface between DSP and memory chip. Among them, DSP processor module uses TI's fixed-point digital signal processor TMS320VC5509A, the processor for the 32-bit fixed-point high-speed digital processor, the maximum operating frequency of 200MHz, chip built-in 64K Bytes ROM, 128K * 16-bit RAM. Comes with USB2.0 FullSpeed interface, you can transfer images, video and other high-speed data. (ADC), clock generator, memory direct access controller (DMA), external memory interface (EMIF), the host interface (HPI), the internal integrated circuit (IC), the internal memory (I/O), and so
First, DSP needs to use the simulator, reads in the primitive image from PC machine, stores in the unit the image data which the DSP assigns, then needs to initialize the image, again carries on the statistics to image each picture element, thus obtains the original map alike histogram, then carries on the histogram adjustment, the computation obtains the new histogram data. This time, again maps the histogram the new storage space, then has completed this time the image enhancement through the DSP digital signal processor. Under this basis, we can summarize the systematic architecture as listed.

- **Reset and clock control module.** In the process of window is generated, each pixel clock will water the generation of the window, but not everyone is effective. For 3*3 window, with 8 neighborhood template convolution, those on the edge of the image pixels without "efficient" window, therefore, only the number of lines is greater than 2 and line number greater than 2 points are valid window. The execution time of the given template calculation module, the gradient magnitude pixel clock delay "effective" pixel clock half cycle. Edge of the binary pixel clock generating process is similar.

- **FIFO and window generation module.** This article uses the FIFO controller and FPGA which ACTEl provides the internal RAM realization. FIFO through two indicator control data read-write and writes the clock and reads the clock separation and this article read-write clock uses in common the picture element clock, when the replacement the read-write address is same, must initialize the read-write address otherwise cannot carry on normally read-write.

- **Template computation and comparison module.** The module calculates $G(x, y)$ in the generated window according to formulas 1, 2. To avoid data overflow, $G_x, G_y$ are the 11-bit signed numbers whose absolute values are determined as follows: If the most significant bit is 1, the result is the inverse of the original number plus 1 and the most significant bit (sign bit) Directly discard the most significant bit (sign bit). Since the following modules compare $G_x$ and $G_y$, obviously saving $G_x$ and $G_y$ will waste a lot of logic units. Therefore, we will extend the result $G(x, y)$ by one bit so that the most significant bits represent the size of $G_x$ and $G_y$. 

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Conclusion

This paper conducts the analysis on the high-resolution image compression algorithm based on the 89s52S single chip microcomputer. The fractal image compression process mainly is approaches the source image using the compression mapping fixed point to complete the image the code, the image reconstruction is realizes through the iteration, this kind establishes above the fractal rationale the image compression method has the very great compression ratio has the widespread application prospect in image compression processing. In this paper, inspired from the imaging and processing system, we propose 89s52S single chip microcomputer based hardware implementation of the compression algorithm. The experiment part proves the effectiveness of the approach. In the later research, we will apply the proposed methodology into more scenarios.
References


