Design of 8 Bit Interpolating Flash ADC Based on CMOS Technology

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ABSTRACT: An 8 bit 1GHz interpolating flash ADC was designed with 0.18um CMOS technology, which was composed of band gap voltage reference, resistance divided network, preamplifier, interpolating resistance structure, high speed latched comparator, bubble code elimination circuit, and encoder circuit. The ADC was simulated at power voltage of 1.8V and sampling frequency of 1GHz, the results showed that the value of the INL and DNL were 0.35LSB and 0.2LSB respectively, SNR was 44.3dB, SNDR was 41.6dB, SFDR was 54.35dB, ENOB was 7.1bit, power consumption was 234mW, and the layout area was 2.36mm².

1 GENERAL INSTRUCTIONS

An interpolating flash ADC was designed based on 0.18um CMOS technology here. The interpolating structure got the favor of people because of its high sampling speed, low power, small chip area and low noise; it was generally used in appliances such as ultra-wideband, digital oscilloscope, LCD, radar, sonar, high resolution image display, military and medical imaging, high performance controller and actuator, and so on.

2 PRINCIPLE AND STRUCTURE

As the traditional flash ADC, the reference voltage was produced by bandgap reference voltage source, which was divided by resistive network, and then these voltages and input signal voltage were amplified simultaneously in preamplifier, compared by comparator, and converted to binary code as output signal through bubble code elimination circuit and encoder. Because of the fully parallel structure, the preamplifier and comparator were needed 2N-1 severally, which greatly increased the power consumption and chip area of the overall circuit.

In this paper design, an 8 bit interpolating flash ADC consisted of bandgap voltage reference (BVR), resistance divided network (RDN), preamplifier (AMP), interpolating resistance structure (Inter R), high speed latched comparator (Comp), bubble code elimination circuit (BCE), and encoder circuit (Enc), such as Figure 1. A series of corresponding resistance strings were connected in series between the adjacent two preamplifiers, and a plurality of reference voltages were divided, which saved most of the preamplifier, reduced the area and the power consumption.

2.1 Bandgap voltage reference
The traditional structure bandgap voltage reference could output accurate voltage, but the power voltage was above 3V at least, and the output of the reference voltage to the minimum is also to 1.2V. To obtain a stable output voltage, the structure should be modified. In this paper, the PTAT current generation structure was used to form the stable voltage with zero-temperature coefficient, as show in Figure 2. The temperature drift coefficient of this bandgap voltage reference was 8.3ppm/℃, the noise was 829μV.

2.2 Resistance divided network
The resistance network consisted of series resistors, which divided the reference voltage into 2N-1 parts; the dividing voltages and input signal, were inputted to the preamplifier together. Due to the differential input structure of the preamplifier, it was easy to generate the feed-through effect, and interfere with
the normal reference voltage, the formula for calculating the feed through voltage:

\[ U = 2^{n-2} \frac{\pi}{2} RC \]  

(1)

Where \( U \) was the feed through voltage, \( f_{in} \) was the frequency of input signal, \( n \) was ADC's bit; \( C \) and \( R \) were the input capacitance and resistance respectively. In order to reduce the deviation, the smaller resistances were used to form the divided network. Thus, the maximum reference resistance is 512Ω.

2.3 Preamplifier and comparator

The linear degree of the preamplifier would affect the number of interpolation zeros, it needed a good match. The appropriate gain of amplifier was beneficial to suppress the offset voltage of the high speed latched comparator. In Figure 3, the preamplifier in this design used open loop positive feedback structure, which had the gain of 38.4dB and unity gain bandwidth of 743 MHz. The series resistors were inserted between the adjacent two preamplifiers to form the interpolation structure, which would increase the numbers of zero, save nearly three quarters of the preamplifier to reduce the power consumption and area. The traditional structure of 8 bit ADC would need 255 preamplifiers, while there were 63.

The circuit of high speed latched comparator was shown in Figure 4. The comparator was controlled by clock signal, it worked at high-level clock signal, and latched at low-level, the response time was 21ps.

2.4 Bubble code elimination and encoder circuit

The metastable state of comparator was that it could not judge to output 1 or 0, when the values of two input signals were too close. The output would be not continuous 0 or 1, but mixed with 0 or 1, such as the bubble in thermometer, so called the bubble code. We used the bubble elimination circuit, as shown in Figure 5; when a code 1 was mixed in a bunch of code 0, it was eliminated with adjacent code 0 through the AND gate.

The ROM encoder was converted to 8 bit binary code in this paper, which had the advantages of compact structure, small wiring area, and small parasitic capacitance, and so on.

3 SIMULATION AND RESULTS

The complete circuit of 8 bit interpolating flash ADC was shown in Figure 6. In the simulation time of 500ns, the output waveforms of 8 bit ADC were completely correct, as shown in Figure 7.

When the supply voltage was 1.8V, the clock signal frequency was 1GHz, the simulation results of static parameters were measured by Matlab, and the
values of DNL and INL were 0.2LSB and 0.35LSB respectively, as shown in Figure 8 and Figure 9.

The dynamic simulation results were shown in Figure 10. SFDR was 54.35dB, SNR was 44.3 dB. According to the relationship at below,

\[ ENOB = \frac{(SNR - 1.76)}{6.02} \]  

Where could be concluded that ENOB was 7.1 bits and SNDR was 41.6db. Through calculation of the overall circuit, its power consumption was 234mw and the layout area was 2.36mm². The layout was shown in Figure 11.

\[ SNR = ENOB \]

To compare with the other three papers in Table 1, the comparison results were shown that the values of INL and DNL were better than other three papers, SNDR and the layout area were superior to the results of the first two papers in the Table 1, and the sampling rate of the interpolation flash ADC designed in this paper had reached 1GS/s, which was higher than the results of the first and third papers. The power consumption of the 8 bit interpolating flash ADC was 234mW.
Table 1. The comparison of ADC parameters.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>W. Wei</th>
<th>K. Liu</th>
<th>L. Yuan</th>
<th>Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>DNL (LSB)</td>
<td>1.01</td>
<td>0.3</td>
<td>0.33</td>
<td>0.2</td>
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<tr>
<td>INL (LSB)</td>
<td>1.92</td>
<td>0.45</td>
<td>0.48</td>
<td>0.35</td>
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<tr>
<td>Area (mm²)</td>
<td>4.35</td>
<td>5.7</td>
<td>2.29</td>
<td>2.36</td>
</tr>
<tr>
<td>SNDR (dB)</td>
<td>41.4</td>
<td>39.2</td>
<td>59.5</td>
<td>41.6</td>
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<tr>
<td>ENOB (bit)</td>
<td>7.1</td>
<td>6.3</td>
<td>9.59</td>
<td>7.1</td>
</tr>
<tr>
<td>Resolution (bit)</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Technology (um)</td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
</tr>
<tr>
<td>Supply voltage (V)</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
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<tr>
<td>Consumption (mW)</td>
<td>97</td>
<td>774</td>
<td>195</td>
<td>234</td>
</tr>
<tr>
<td>Sampling rate (GS/s)</td>
<td>0.5</td>
<td>1.0</td>
<td>0.1</td>
<td>1.0</td>
</tr>
</tbody>
</table>

4 CONCLUSIONS

An 8 bit 1GHz interpolating flash ADC was designed here, it not only had the high conversion speed of the traditional flash ADC, but also saved nearly 3/4 of the preamplifier because of its interpolation structure, which had reduced the power consumption and saved the area. Through comparison, we could see that the interpolating flash ADC designed in this article were relatively good in many ways, such as speed, static or dynamic characteristics, the layout area and power consumption. In the future, the design will be finally verified and taped out.

5 ACKNOWLEDGMENTS

This project was funded by the 2008 Heilongjiang University Youth Science Foundation Project (QL200808), and the Heilongjiang Provincial Education Department Key Laboratory Scientific Research Project of Electronic Engineering (DZZD20100034).

REFERENCES