Design of the CCD-TCD2964BFG Drive and Sampling Based on FPGA

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ABSTRACT: This technology is mainly focused on the charge coupled device (CCD)TCD2964BFG as image sensor and using AD9826 as sampling chip, which introduces a design of driving and sampling circuit based on the FPGA of Altera Corporation. It discusses the design of driving and control timing by using FPGA chip EP4CE30F23C7N technology. Then it describes the design of the CCD driver board and the CCD mounting board in detail. This is a pivotal design to high-precision measurement, color image scanning and so on. Its highest accuracy can be reached 4800DPI with high resolution when it works and its output signal can be more reliable, more stable by being processed by AD9826, so it is very important for high-precision measurement, color image scanning ,etc. While making it into sub-circuit board physical model by using integrated circuit form, meanwhile, it’s very convenient to connect with a variety of FPGA core boards and it can be applied on various occasions by outgoing interface signals. The design is known for its flexibility, high integration, easy to update, convenient to apply and so on. The observed results indicate that the design of driving timing and circuit can meet the normal demands for the color linear CCD.

KEYWORDS: FPGA; Color linear CCD; Drive and sampling ;Image scanning; Integrated circuit.

1 INTRODUCTION

Charge couple device(CCD) is a new type of semiconductor devices which can transfer optical signal into the electrical signal well through electric charge for achieving photoelectric conversion[1]. It is widely used in the imaging field for its advantages such as high accuracy, good resolution and low power consumption, etc[2]. However, there are few designs for color linear array CCD, and they have a broader range of applications than non-color linear CCD with the characters of high effective pixel, high-resolution, multi-precision mode. So, the driving design for color linear CCD is very meaningful.

In addition, the drive timing sequence of color linear CCD we chose has a little complicated. The key of driving high-speed CCD is that we need to get stable driving and control timing. That is to say we must optimize codes and provide some special requirements for the circuit board design. The drive circuit of early CCD is implemented by conventional digital circuit chip such as EPROM,IC, etc. But there are some disadvantages through using early driving methods such as debugging difficult, inflexible, large drive circuit area and so on. Nowadays, we can make full use of FPGA’s ‘programmability’[3], so, a method of driving and sampling pulse based on FPGA is introduced in this paper. FPGA with the characters of high integration, flexibility re-configurable, good portability and saving space of PCB board. At the same time, the product with development cycle shorter, easy to update based on FPGA is the trend of market development[4].

2 THE PRINCIPLE AND ANALYSIS OF TCD2964BFG

CCD is the media converter component part integrated by the photosensitive element. The color CCD image sensor in this design is TCD2964BFG of Toshiba in Japan which is a high sensitive and low dark current 21360 elements X 6 line CCD color image sensor. The sensor is designed for scanner. It provides a 192 lines/mm (4800DPI) across a A4 size paper and it is operated by 5V pulse and 12V power supply.
Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark conditions) calculated by the following procedure. So the output waveform of the color CCD image sensor is shown as Figure 1.

![Figure 1. The output waveform of TCD2964BFG.](image)

Then the timing sequence driving figure of the TCD2964BFG is shown in Figure 2[5].

![Figure 2. The timing chart of TCD2964BFG.](image)

As we can see, the timing driving is made up of Timing chart 1 to Timing chart 4. To make the CCD work normally, we need to follow a certain timing constraints. In addition, the timing driving circuit should provide 9 timing pulse. They are storage pulse ST, shift pulse SH1 to SH4, clock pulse $\phi_{1A,B}$ and $\phi_{2A,B}$, reset pulse RS and mode select pulse SW. Its effective units can reach 10680*4 pixels that contain odd and even columns which are output by the ports of OS1, OS2 and OS3.

In some non-contact measurement systems, the CCD data plays a very important role in the measurement precision. The FPGA chip EP4CE30F23C7N is used in the timing driving design. In the design we chose the overall clock frequency of the FPGA chip is 50MHZ, we will choose the typical value of each pulse as its cycle. Such as the typical value of $\phi_{1A,B}$ pulse is about 1MHZ, the typical frequency of RS pulse is 2MHZ and so on. We can achieve them by frequency division to the global clock frequency[6].

3 THE PRINCIPLE AND ANALYSIS OF AD9826

In view of the TCD2964BFG, the Correlated Double Sampler (CDS) chip AD9826 is used in the design. The AD9826 is a complete analog signal processor for imaging applications. It features a 3-channel architecture designed to sample and condition the outputs of trilinear color CCD arrays. Each channel consists of an input clamp, Correlated Double Sampler (CDS), offset DAC, and Programmable Gain Amplifier (PGA), multiplexed to a high-performance 16-bit A/D converter. It operates from a single 5V power supply. The timing diagram of AD9826 is shown as Figure 3[7].
4 THE DESIGN OF DRIVING CIRCUIT

Nowadays, the circuit boards are mainly implemented by the printed circuit board (PCB)[8]. The software development platform of PCB is Altium Designer 6.9 in this design. To implement the high speed color CCD driving we must make sure the rising and falling edge fast enough. According to the requirement of the rising and falling time and the capacitance of the CCD the resistance R can be calculated. Some measures should be taken to make the sum of output resistance of the driver and the serial resistor equal to R. Taking into account the help of device handbook[7], we design the driving circuit schematic that is shown in Fig. 4.

Considering the color CCD is 32 pin CLCC package, we design a sub-circuit board for it to protect it easily. So the schematic diagram of PCB is shown as Figure 5.

5 EXPERIMENTAL RESULTS

The soft development tool of CCD signal simulation is Quartus II. Then using Verilog HDL as programming language. At last, in order to verify the correctness and effectiveness of the method proposed in this paper, some experiments need to be done.

First, after the code is compiled without error, the sof file is download to the FPGA board through JTAG interface and the simulation result of the various pulses of CCD and AD9826 is shown as Figure 6. Then, the practical PCB test was done, the test board is shown in Figure 7. At last, we use the oscilloscope to watch and record the waveform. Figure 8 shows the diversification of the waveform of the CCD when we weaken the light of the CCD successively.

Figure 3. The 3-Channel CDS mode timing.

Figure 4. The schematic of driving circuit.

Figure 5. The schematic of PCB.

Figure 6. The simulation waveform of TCD2964BFG and AD9826.
6 CONCLUSIONS

By analyzing principle and features of the color CCD sensor and AD 9826, a design of driving timing and circuit is proposed in this paper and a kind of driving timing method and circuit are discussed. The application of color linear CCD with multiple working modes has a great significance and it is critical to achieve high performance for the CCD imaging systems. To make full use of FPGA’s programmability, software and hardware all use programming so that make the design flexible and easier to modify. Experimental results indicate that the design for the TCD2964BFG gets perfect results, can meet the requirements of the color CCD well. This builds the foundation of next-stage research for the measure system, file scan and spectroscopy, etc, and the driving design has a certain reference for the other color linear CCD in the future.

REFERENCES