Analysis Method of Compound ADC Modeling

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Abstract. A new type of ADC with a precision of 10-bit and a sampling rate of 250M is implemented by modeling. The new composite ADC proposed in this paper achieves high power consumption and reduced area with high accuracy and medium speed by combining the advantages and disadvantages of pipeline ADC and SAR ADC. In this paper, the system modeling and simulation verification are carried out for the new composite structure ADC. In the premise of considering many non-ideal factors, the input end access 36.6MHz input signal, sampling clock frequency using 250MHz, the system can achieve SNR = 58.5dB, SFDR = 68.8dB, ENOB = 9.3 and other design indicators. The design of this system model provides the direction for the determination of important module design parameters in the actual circuit-level design system. At the same time, it provides the basis for analyzing the influence of various non-ideal factors on static and dynamic characteristics and the ADC energy in ADC system design.

Introduction

ADC as the connection of analog circuit and digital circuit channel, always cannot be replaced, along with the rapid development of the integrated circuit industry, the performance of the chip especially in speed, power consumption has put forward higher requirements, on the same ADC performance requirements are also rising. The traditional structure of ADC has been unable to meet the needs of today's design, the new design has emerged as the times require. In this paper, according to the needs of the current development, combined with the advantages and disadvantages of the traditional ADC structure, a new composite structure of ADC is proposed, and the ADC of this new type is modeled, simulated and verified on the Matlab Simulink platform.

The Proposed Structure of Composite ADC

According to this design index, 200MHz 10-bit ADC, if the use of Pipeline ADC alone to achieve, assuming the conversion accuracy of each level of 2.5bit, you need 5 levels of cascade, you can achieve the accuracy of 10-BIT. Since the Pipeline ADC is working in parallel, the speed is not a problem, but the cascade of 5 levels, according to the traditional structure, requires 5 operational amplifiers, 30 comparators and several logic circuits and capacitors[1]. And for the use of traditional successive approximation structure ADC to achieve the same design specifications need 2048 units of capacitance, in addition to the traditional SAR structure to achieve 250M speed 10bit accuracy, each conversion time of 400ps, so short time for the traditional structure of the SAR ADC is difficult to achieve[2]. In this paper, we propose a composite structure ADC to alleviate the contradiction between the various indexes. According to the design index, this paper proposes a two-step Pipeline ADC structure and a 6-bit SAR ADC structure. The composite structure requires 13 comparators, two op amps, and 256 units of capacitance. This shows that the same performance under the conditions of the composite structure can save most of the area and power consumption. In addition, you can use the digital correction algorithm of the pipelined ADC for correction. However, in the case of ensuring
sufficient conversion accuracy of the remaining bits, the correct connection between the pipeline structure and the successive approximation structure is the difficulty of the design.

![Figure 1. Structure of compound ADC](image1)

The structure of the composite structure ADC proposed in this paper is shown in Figure 1. The figure consists of four parts: the first part is the pipeline structure level using two-level structure of each 2.5bit, to achieve 4bit effective accuracy; the second part is the approximation of the structural level, to ensure the accuracy of the front 4bit 6bit conversion accuracy, so the entire ADC to achieve 10bit conversion Accuracy. Clock generation module is used to generate the entire ADC clock signal, where the clock signal frequency to 250MHz. And the last part is digital correction logic and digital code output.

Establishment of Simulation Model of Composite Structure

For the structure proposed in the chapter 2, the behavior level modeling design is carried out by using matlab Simulink platform. A number of non-ideal factors are considered in this design to ensure that the entire ADC modeling is closer to the actual circuit level implementation. The core modules will be analyzed and introduced in accordance with the overall structure of the composite structure ADC.

Sample and Hold Module Modeling

The sample retention module is the most front-end module of ADC, and it has an influence on the performance of each module and the whole. Therefore, it is very important to consider the non-ideal factors for sampling retention. The non-ideal factors in the sampling maintenance circuit mainly include: clock jitter, sampling noise, transport noise, switching noise, limited gain of transport, limited bandwidth of transportation, capacitance mismatch, etc[4].

![Figure 2. Sample and hold module modeling](image2)

The sample retention structure is modeled as shown in figure 2. Clock jitter is a result of the sampling clock is not ideal, resulted from random jitter along the deviation between the actual clock along and ideal clock, this deviation is a stochastic process is within a certain range of random size. Therefore, a gaussian random number is used to simulate the clock jitter.

The second is the noise from sampling and transportation, and the noise in the sampling is mainly derived from the KT/C noise, which generated by the pilot resistance of the sampling switch and the sampling capacitor[5].

The final factor is limited gain error and limited bandwidth error. They are caused by the limited gain and limited bandwidth of the transport. The closed-loop transfer function of the switching capacitor operation amplifier is shown below[4].

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\[
\frac{v_{\text{out}}}{v_{\text{in}}} = \sum_i^n c_i \left( \frac{Af}{1+Af} \right) = \sum_i^n c_i \left( \frac{1}{1+\frac{1}{A\beta}} \right)
\]  

(1)

Among them, \(A\) is to carry out the loop gain, \(f\) is the feedback coefficient, \(CS\) is the sampling capacitor, \(Cf\) is the feedback capacitor, and the gain error is

\[
\Delta_{\text{gain}} = \frac{1}{\beta A} \approx \frac{1}{\beta A}
\]  

(2)

Assuming that the transport is a first-order response, \(\omega_{3\text{dB}}\) is the open loop 3dB bandwidth, and the open loop transfer function is as follows:

\[
A(s) = \frac{A}{1 + \frac{s}{\omega_{3\text{dB}}}}
\]  

(3)

In the upper formula \(\tau = (\beta \omega_{\text{ta}})\), \(\omega_{\text{ta}}\) is the unit gain bandwidth, which will be converted to the time domain.

\[
h(t) = \sum_i^n c_i \left( 1 - e^{-\frac{t}{\tau}} \right)
\]  

(4)

According to the above formula, the limited bandwidth error is

\[
\Delta_{\text{bw}} = e^{-\frac{t}{\tau}}
\]  

(5)

\(T\) is the working cycle time of the switching capacitor operation amplifier. In the modeling in figure 2, the above error has been added to the sampling circuit by using the Gain module.

**Sub-ADC Module Modeling**

The function of the sub-ADC module is to roughly quantize the input signal to obtain a coarse quantized digital output code. The core module in the sub-ADC is the array of comparators, and the most important non-ideal factor in the design of the comparator is the offset voltage. Figure 3 shows the sub-ADC Simulink modeling, which mainly considers the impact of the comparator’s offset voltage on the sub-ADC.

![Sub-ADC module modeling](image)

**Sub-DAC Module Modeling**

The function of Sub-DAC module is to convert the output digit code in sub-ADC to the corresponding analog signal value. General circuit are used switched capacitor amplifier MDAC module to achieve DAC, subtraction and redundant amplification[6]. The Simulink modeling of the Sub-DAC is shown in Figure 4, taking into account the effect of capacitance mismatch and noise on the Sub-DAC.
SAR Logic Module Modeling

The main function of SAR Logic is to reset the circuit. The digital output code of the corresponding bit is generated according to the output of the comparator in each cycle, and the digital output code of the sync latch circuit until all the digital codes are output after the entire conversion process. The SAR Logic modeling in this paper is designed using the Stateflow tool provided by Matlab, as shown in Figure 5. This structure can implement the corresponding digital logic function.

Overall Structure and Simulation of Compound ADC Model

Figure 6 shows the overall structure of the composite ADC, the input side of the 250MHz input of the sinusoidal input signal as a test signal, while the other modules in the model set the corresponding parameters, such as op amp gain of 80dB, bandwidth of 900MHz. Other non-ideal factors such as noise, offset, mismatch and other non-ideal factors do not consider, so that each module is similar to the ideal situation, the behavior model simulation.

Output through Matlab FFT analysis, simulation of complex static characteristic and dynamic characteristic of ADC, get compound ADC static characteristic and dynamic characteristic and static characteristics are shown in Figure 7. From the simulation results can be seen that the composite ADC design is feasible. Due to no consideration of noise, capacitance mismatch, gain error, the establishment of errors and other factors, so the circuit operating characteristics close to the ideal situation.
Non-ideal factors such as the offset voltage of the comparator, the mismatch of the capacitance, the presence of noise in the module, etc. are set according to the actual possible range. Using Matlab to process the output results to get the corresponding dynamic and static characteristics shown in Figure 8.

![Figure 8. Simulation of static characteristics of compound.](image)

**Conclusion**

In this paper, a new composite ADC is proposed, and the feasibility of this composite ADC is verified by Matlab Simulink tool. Through comparing with the traditional structure, this new type of composite structure of ADC can set a better compromise in the ADC speed, accuracy, power, area and other important indicators. On the premise of guarantee the high accuracy, moderate conversion speed, greatly reducing power consumption and area.

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**References**


