A 10Bit Small Area Low Power Pipelined SAR ADC Used in CMOS Image Sensor

Zhen Li and Dongmei Li

ABSTRACT

This paper presents a novel architecture to achieve a low power and small area pipelined SAR-ADC which used in a CMOS image sensor. The sub-SAR ADC is a key module to lower power consumption and design complexity. The high-resolution first stage, the half-gain MDAC and the dynamic comparator are adopted to improve the linearity and to reduce the power. This pipelined SAR ADC is fabricated in 180nm CMOS technology with active area of only 140um×280um. The ADC achieves 60.37dB signal-to-noise and distortion ratio (SNDR) and 76.37dB spurious free dynamic range (SFDR) with 3MHz frequency input. The power dissipation is 9.8mW in typical case under 2.8V supply.

KEYWORD: Pipelined SAR ADC; small area; low power; half-gain MDAC; dynamic comparator

INTRODUCTION

Recently CMOS image sensors have been widely used in consumer electronics, including mobile phones, digital cameras, etc. A CMOS image sensor mainly consists of a pixel array, readout circuits, a Programmable Gain Amplifier (PGA), an Analog-to-Digital Converter (ADC) and a Digital Signal Processor (DSP) (Li X, 2008). The block diagram is shown in Fig. 1. The ADC plays a key role in converting the image signals, whose frequencies span from DC to a few MHz. Pipeline structure is generally employed in chip level to satisfy the readout speed as well as a moderate resolution. However, the traditional pipeline structure brings extra power consumption and non-ideal factors, such as aperture errors, sub-ADC errors and nonlinear errors. Many works such as (Xue, et al, 2014) and (Lee B G, et al, 2008) have been done to eliminate these errors. The deficiencies above limit its application in consumer electronics, which have strict requirements of power consumption and area.

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On the other hand, successive approximation register (SAR) ADC has surpassed pipeline structures in terms of energy efficiency and it requires a minimum number of analog components, typically a comparator, a capacitor array, and SAR control logics (Wang Q, et al, 2014).

Portable and wearable devices is the growing trend in consumer electronics. To maximize the battery life and be convenient to carry, energy-efficient and small area ADCs are needed. So the merits of pipeline and SAR structure can be integrated to meet the above demands. This paper presents a novel

![Figure 1. The block diagram of a CMOS image sensor](image1)

![Figure 2. The Proposed ADC Architecture](image2)

ADC used in CMOS image sensors that combines the pipeline and SAR structure together to relieve above problems. In this structure, two medium resolution SAR ADCs are used as the sub-ADC to replace the traditional flash type. The first stage has a high resolution multiplying digital-to-analog converter (MDAC) to lower the power and improve the linearity. Furthermore, a half-gain technique is proposed to reduce ADC nonlinearity due to finite op-amp gain. As this circuit is aimed for applying in industrial product, cost and stability matters most. So the mature 180nm CMOS technology is adopted and the area should be as small as possible.

Section II describes the considerations in determining the whole architecture including theoretical derivation and detailed implementations of key blocks. Section III shows the circuit performances and Section IV gives the conclusion.

CIRCUIT DESIGN AND IMPLEMENTATION

Proposed ADC Architecture

Fig. 2 illustrates the proposed ADC architecture, mainly containing four parts: a 5b MDAC, a 6b SAR ADC, the 1b digital error correction and clock control block. The first stage 5b sub-ADC with 1b redundancy reuses the MDAC input sampling capacitor array as its capacitor digital-to-analog converter (CDAC) to implement a SAR sub-ADC. The half-gain MDAC is employed to amplify the residue from the first stage. Avoiding the need for more pipeline stages, the second-stage also employs the SAR architecture to achieve a 6b resolution. The timing control block is used to generate the clock signals and the digital error correction block combines the data from two stage. So, a 10b output code is obtained.

The timing diagram of the ADC is shown in Fig. 3. During phase CLK_S, the op-amp resets and the first stage samples the input signal at the bottom plate with the bootstrapped switch. After sampling, the first stage’s comparator is activated to
perform conversion and starts to generate m bits (m is the first stage resolution). The charge on top plate of the capacitor array is then transferred to the feedback capacitor of the op-amp to amplify the residual voltage by a factor of \(2^{m-1}\) during phase CLK_H. The first stage samples the new input again while the second stage begins to convert the residue signals.

**5b MDAC Architecture**

Fig. 3 shows the single-ended circuit detail of the 5b MDAC architecture. The actual implementation is fully differential. In a traditional pipeline ADC, a 1b or 1.5b flash sub-ADC is usually employed. (Yang W, et al, 2001) has proved that a large resolution (m) in the first stage is very beneficial for the ADC performance as a whole. Here the effects of the stage resolution on the linearity, power and noise are analyzed.

The differential non-linearity (DNL) of the ADC is used to evaluate the linearity and it is mainly caused by the capacitor mismatch in the first stage. Equation (1) shows the relationship:

\[
DNL \propto \frac{K \cdot 2^{\frac{N}{m}}}{\sqrt{C_{\text{total}}}}
\]  

(1)

Where \(C_{\text{total}}\) is the total capacitance of the sub-converter array and determined by the SNDR requirement. \(N\) is the total resolution of the architecture and \(m\) is the first stage’s resolution. Obviously DNL is improved by a factor of \(\sqrt{2}\) for every one bit increase in the first stage and is also improved by \(\sqrt{2}\) for the doubling of \(C_{\text{total}}\).

Figure 3. Implementation of 5b MDAC.  
Figure 4. Consideration in choosing the unit capacitor.

However, if the high resolution is implemented with the traditional flash ADC, a power-hungry front-end sample-and-hold(S/H) is a must to avoid aperture errors between MDAC sampling and sub-ADC decision. Besides, \(2^m\) comparators are needed to implement an m-bit flash sub-ADC. All of these make it difficult to implement a large stage resolution. The SAR ADC overcomes the problem perfectly. The sampling path mismatch and aperture errors are eliminated by reusing the input sampling capacitor array of MDAC as sub-SAR ADC’s CDAC. Therefore, they share the same sampling path. And sub-SAR ADC is integrated into MDAC by just connecting one comparator to the top plate of the input capacitor array, thus reducing the number of comparators from 32 to 1 and alleviating the design complexity.
A large unit capacitor can reduce the capacitor mismatch with an increasing cost of the area. So the value of the unit capacitor is carefully considered to make a balance between the linearity and the area. Here a theoretical analysis is proposed to determine the unit capacitor. Assuming an N-bit CDAC constituted by 2N unit capacitor Cui. All unit capacitors are subject to independent and identical Gaussian distribution. uo is the output voltage on the top plate of the capacitor array and u_ref is the reference voltage. The distribution of uo is used to measure the INL distribution. As described in (2) and (3):

\[
\frac{u_o}{u_{ref}} = \frac{\sum_{i=1}^{\text{code}} C_{ui}}{\sum_{i=1}^{2^N} C_{ui}} \tag{2}
\]

\[
\frac{du_o}{u_o} = \frac{d\left[\sum_{i=1}^{\text{code}} C_{ui}\right]}{\sum_{i=1}^{\text{code}} C_{ui}} - \frac{d\left[\sum_{i=1}^{2^N} C_{ui}\right]}{\sum_{i=1}^{2^N} C_{ui}} \tag{3}
\]

Where code means the converted digital data and \(\sigma_{cui}\) is the standard deviation of \(C_{ui}\). Equation (3) is acquired through taking the derivative of (2). As \(\text{dCui}/\text{Cui} \ll 1\) satisfies the conditions, dCui also obeys the Gaussian distribution. According to the rules of Gaussian distribution, get (4):

\[
\frac{\sigma_\text{code}}{u_o} = \frac{\sigma_{C_{ui}}}{u_o} \sqrt{x} \left(1 - \frac{1}{2^N}\right) \cdot \text{code} + 1 \left(1 - \frac{1}{2^N}\right) \cdot \left(2^N - \text{code}\right) \tag{4}
\]

\[
u_o \approx u_{\text{ref}} \cdot \frac{\text{code}}{2^N} = \text{code} \cdot 1\text{LSB} \tag{5}
\]

The relationship in (4) and (5) can be plotted to display clearly. Fig. 4 shows the relationship between the linearity and the unit capacitor. Here, X-axis is the value of \(u_o/2^N\), namely the percentage of output voltage to reference. Y-axis is the resolution of SAR ADC. Z-axis represents the value of \(\sigma_{\text{code}}/(\sigma_{C_{ui}} \cdot 1\text{LSB})\) to measure the output voltage error caused by capacitor mismatch. It can be seen that the output voltage error is becoming worse with the increase of the resolution. And when resolution is stable, different codes correspond to different output voltage error and the error is the biggest when code = \(2^N/2\). So this relationship indicates that the resolution of the first stage is not the bigger the better and 5b is an optimum trade-off. More importantly, it provides a way to determine the unit capacitor. For example, \(\sigma_{C_{ui}} = 2 \cdot \frac{\sigma_{C_{ui}}}{C_{ui}} \cdot 1\text{LSB} \cdot \frac{u_o}{C_{ui}}\) can be obtained from the foundry and the biggest \(z\) can be obtained from Fig. 4. To satisfy the range of INL index, it can be determined that which \(C_{ui}\) makes \(\frac{u_o}{C_{ui}}\) minimum from the foundry technical documents. When \(N = 5\), 10\(\text{fF}\) is suitable for the unit capacitor to meet the demands of INL < 0.5LSB. Here the 5b SAR ADC is not thermal-noise-limited, so \(kT/C\) noise has little effect in this process.

**Comparator Design**

When designing a comparator of ADC for CMOS image sensors, the offset matters most. However, it is not a fixed value and hard to eliminate in industry. In
order to reduce the influence of offset, an energy-efficient dynamic comparator with a preamplifier shown in Fig. 5 is adopted in this design (Chan C, et al, 2011).

The comparator includes a preamplifier and a dynamic latch-type sense amplifier. With the gain of about 20, the preamplifier is placed before the dynamic latch alleviating the comparator offset. Two cross-coupled transistors is added to reduce the kick back noise. A pair of PMOS transistors consists of the loads of the preamplifier so that the size of them should be carefully designed. Decreasing the size of the PMOSs is good for speed, but it will also reduce the gain of the amplifier, which is bad for the offset and noise of the second stage. This comparator works at either reset phase or compare phase. What is worth noticing is that the settling time of the comparator is different in different stage. From the timing diagram in Fig. 2, it is obvious that the first stage’s comparator has a high demands for the comparing time. Therefore the size of the transistors can be different in different stage’s comparator.

![Figure 5. Dynamic comparator with preamplifier.](image)

### Half-gain MDAC

Fig. 3 shows the single-ended schematic diagram of the 5b MDAC. Here, the op-amp gain of 16 found in conventional architecture is reduced to 8. This helps to further reduce the op-amp power consumption and significantly improves the ADC linearity. The stage amplifier employs the closed-loop feedback structure with switched-capacitor. The closed-loop gain is \( \frac{C_{in}/C_f}{1+1/\beta} \) and the feedback \( \beta = C_f/(C_{in} + C_f + C_p) \). Ignoring the parasitic capacitance, the half-gain technique increases the feedback from \( \frac{1}{17} \) to \( \frac{1}{9} \). The closed-loop bandwidth is proportional to \( \beta C_{in}/C_{op} \). Assuming the demand for the bandwidth stays the same, transconductance \( g_{in} \) is reduced by half. Therefore, the power consumption is significantly lowered.

The linearity is improved according to the following analysis. The maximum absolute value of DNL caused by first-stage op-amp finite gain is described in (6)

\[
|DNL|_{max} \propto \frac{2^{V_{sat}}}{A\beta} \tag{6}
\]

The almost two-fold increase in \( \beta \) reduce the absolute DNL value by half so that the linearity is improved. Besides, the voltage swing of the op-amp output is reduced by half, which lowers the design complexity of the op-amp and allows us to enhance the op-amp gain under the same condition. In return, the gain enhancement lower the finite gain error. Though the decreased voltage swing
reduces the LSB size for the second stage, it affects the total performance little because 6b SAR is not thermal-noise-limited. However, a further reduction in the gain, e.g., a quarter gain, greatly reduces the LSB size and the thermal noise becomes to dominate (Lee C & Flynn M P, 2011). Outweighing the disadvantages to the second-stage, a half-gain implementation is appropriate.

**Second-Stage 6b SAR ADC**

The second stage is similar to the first sub-SAR ADC and quantizes the first-stage output Vres to 6b. Here the reference voltage is reduced half compared to the first stage to compensate for the half-gain MDAC. What is worth noticing is that the second stage has sufficient time to sample and quantize compared to the first stage. So low power becomes the most important factor. Here the comparator without preamplifier discussed in Section II-C is employed. What’s more, the second stage contributes little noise to the whole circuit for the existence of the stage amplifier. Here the noise from capacitor mismatch and comparator noise have little effect in this stage. So the requirement analyzed in Section II-B can be further relaxed and the unit capacitor can be reduced by half, which leads smaller area.

**Digital Error Correction**

This architecture is calibration-free for two reason. Firstly, the half-gain MDAC technique helps to realize a high open-loop gain as well as to meet the same requirement of the closed-loop bandwidth and DNL. Thus, the demand for the gain calibration can be eliminated. Secondly, the stage resolution is relatively small compared to moderate resolution (10-12b) SAR ADCs. So the capacitor mismatch can be well decreased by carefully choosing the unit capacitor according to analysis in Section II-B. Therefore, capacitor mismatch calibration is not needed in both stages. Here the digital error correction is employed to compensate the offset from the comparator in both stages. Considering the effect of offset, the 10b codes are generated through the digital error correction with 1b overlapping. The last bit of the 5b first stage code and the first bit of the 6b second stage code are combined into one bit with digital addition.

**CIRCUITS PERFORMANCE**

The proposed low power and small area pipelined SAR ADC is used in a CMOS image sensor in industrial product and fabricated in 1P3M 180nm CMOS technology. As the CMOS image sensor is applied in consumer electronics, the area is strictly limited. In this architecture, traditional capacitors of MIM type are replaced with MOS cap, which has good dynamic matching and large unit-area capacitance. In this way, the area cost is sharply reduced. The core area of ADC layout shown in Fig. 6 is only 140μm × 280μm, about 0.04mm². The area is significantly decreased. The ADC along with the CMOS image sensor are supplied with 2.8V voltage. The total power consumption, including consumption from reference voltage, which occupies a large power consumption in actual work, is 3.5mA. The simulation results at Nyquist frequency are shown in Fig-7. The key performance is summarized and compared
with traditional pipeline ADC of previous published works used in this area in TABLE I

![Image of circuit diagram](image)

**Figure 6. The Layout of Proposed ADC.**

![Image of spectrum graph](image)

**Figure 7. The ADC output spectrum.**

**CONCLUSION**

In this paper, a low power and small area 10b new pipeline ADC architecture is presented. The proposed ADC combines the advantages of the pipeline structure and SAR structure through replacing traditional flash-type sub-ADC with SAR ADC. Both of high resolution in the first stage and half-gain MDAC technique help to achieve better power efficiency and linearity. The area of the ADC is 0.04 mm$^2$ and power consumption is 9.8 mW with the 2.8V power supply. The pipelined SAR ADC achieves an ENOB of 9.74 bit for 511 x 640 input. The performance of the ADC is fully suitable for the CMOS image sensor

**TABLE I. PERFORMANCE COMPARISON.**

<table>
<thead>
<tr>
<th></th>
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<th></th>
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</thead>
<tbody>
<tr>
<td>Architecture</td>
<td>Pipeline</td>
<td>Pipeline</td>
<td>Pipelined SAR</td>
</tr>
<tr>
<td>Technology</td>
<td>180nm CMOS process</td>
<td>180nm CMOS process</td>
<td>180nm CMOS process</td>
</tr>
<tr>
<td>Area</td>
<td>0.8 mm$^2$</td>
<td>7.28 mm$^2$</td>
<td>0.04 mm$^2$</td>
</tr>
<tr>
<td>Power Supply</td>
<td>3.3 V</td>
<td>3 V</td>
<td>2.8 V</td>
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<tr>
<td>Power Consumption</td>
<td>33 mW</td>
<td>230 mW</td>
<td>9.8 mW</td>
</tr>
<tr>
<td>Resolution</td>
<td>10 bit</td>
<td>14 bit</td>
<td>10 bit</td>
</tr>
<tr>
<td>Sampling Frequency</td>
<td>50MHz</td>
<td>100 MHz</td>
<td>6 MHz</td>
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<tr>
<td>SNDR</td>
<td>58.28 dB</td>
<td>72.2 dB</td>
<td>60.37 dB</td>
</tr>
<tr>
<td>ENOB</td>
<td>9.39 bit</td>
<td>11.7 bit</td>
<td>9.74 bit</td>
</tr>
<tr>
<td>SFDR</td>
<td>64.67 dB</td>
<td>91.1 dB</td>
<td>76.37 dB</td>
</tr>
</tbody>
</table>

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