INTRODUCTION

OFDM has been accepted as an efficient technique for high speed digital communications due to its highest spectral efficiency, low complexity in dealing with large delay spread channels [1], and simple scheduling methods of radio resources. Therefore, OFDM is the foundation of numerous current communication standards for both wireless and wire-line applications [2], such as IEEE 802.11 protocol family for wireless local area network [3], and so on. For the traditional OFDM transmitters, the time domain baseband digital signal is generated from frequency domain mainly by IFFT, up-sampling and interpolation LPSF modules. At the receiver side, after down-conversion and analog-to-digital conversion (ADC), FFT is employed to demodulate the original signal. Among the aforementioned procedures, IFFT and FFT are the key parts of OFDM system ever since OFDM was first proposed by Weinstein and Ebert [4] in 1970s and applied in practice.

The current FFT (or IFFT) processors are mainly based on Cooley and Tukey’s structure [5]. However, after closely inspecting these structures, we observe that they have three obvious limitations when implementing OFDM transmitter. First, the transformed data length should be a power of 2, which constrains the number of OFDM sub-carriers also to be a power of 2. Second, FFT requires a large number of arithmetic operations and thus its hardware complexity is very high. Third, it always takes a long time for the FFT processors to achieve the transform, which lengthens the latency for the transmitter to start outputting its time domain data. Typically, the FFT operating time is dozens of microseconds [6].

ABSTRACT: Traditional orthogonal frequency division multiplexing (OFDM) transmitter is implemented by exploiting inverse fast Fourier transform (IFFT), up-sampling, and low pass shaping filter (LPSF) modules, which occupy a large number of hardware resources and severely lower down the operation speed. To address these limitations, we propose a novel OFDM transmitter architecture, by which the aforementioned modules can be discarded and replaced with some simple switches. In the proposed architecture, direct digital synthesis (DDS) method is employed to generate digital sub-carriers and to transform OFDM data from frequency domain to time domain. Through some sophisticated simplifications, the proposed architecture can avoid using multipliers and remarkably save hardware resources. Finally, comparative experiments are carried out on field programmable gate array (FPGA) platform which demonstrates that our DDS-based architecture saves more than half of the hardware resources and doubles the achievable maximum frequency compared with traditional structure.

Keywords: DDS; IFFT; OFDM Transmitter

1 INTRODUCTION

Novel Low-complexity OFDM Transmitter Without IFFT and Multiplier

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In view of the aforementioned limitations, we propose an alternative DDS [7] based OFDM transmitter architecture to modify the traditional IFFT-based structure. The implication of the proposed architecture is to numerically construct all the sub-carriers by DDS modules, and then add all the modulated DDS signals together to generate the time domain digital data. Based on DDS method, the proposed architecture can be optimized by making full use of OFDM signal’s two distinctive characteristics, i.e., first all the sub-carriers have the same frequency interval, and second all the frequency domain data belongs to a communal set with small number of elements. By using the first characteristic, we make all the DDS modules share a small number of read-only memory (ROM) banks, which consume the ROM amount even less than IFFT module. Per the second characteristic, we use simple switches to substitute the multipliers which are traditionally needed to modulate the sub-carriers by frequency domain data. The reason for this and how to substitute multipliers for switches will be explained in the body of this paper. The above two optimizations dramatically reduce system hardware complexity.

Meanwhile, it is proved that the generated time domain data by DDS principle can automatically conforms to OFDM baseband digital signal’s properties, such as orthogonal and bandwidth constrain. Therefore the LPSF, which also consumes multipliers, becomes dispensable in the proposed architecture. As a result, the proposed transmitter does not need multipliers any more, which enables higher system operating speed. Furthermore, since the proposed architecture is highly parallelized, if implemented on FPGA it is capable of outputting the transformed time domain data one by one per clock cycle soon after the frequency domain data has been input to system. This parallelism eliminates the system latency problem introduced by the IFFT-based structure. The foregoing optimizations and relevant advantages of the proposed architecture can be summarized as the contributions of this paper. Although some works [6,8,9,10,11] have mentioned using DDS to implement OFDM system, they neither simplified the OFDM transmitter’s architecture to the extent that multipliers can be discarded, nor identified the noticeable advantages of DDS-based architecture. Since the DDS-based architecture is quite parallel, the proposed OFDM transmitter is especially suitable for implementation on FPGA.

The rest of this paper is organized as follows. Section 2 gives a brief overview of OFDM transmitter, which leads to the primary DDS-based architecture. Since the primary architecture is still complicated, in Section 3 some approaches are further investigated to simplify it. In Section 4, experiments are carried out on FPGA to verify the performance of the proposed final OFDM transmitter architecture. In Section 5, we prove the orthogonality of the signals generated by the proposed architecture, and analyze its spectrum characteristic. Finally, Section 6 concludes this paper.

2 OVERVIEW OF OFDM TRANSMITTER AND THE PRIMARY DDS-BASED ARCHITECTURE

Figure 1 shows the diagram of traditional OFDM transmitter. The information data is first encoded, and then the interleaved data is modulated and combined with pilot symbols. After serial to parallel conversion, the symbols are performed by IFFT, up-sampling and LPSF as shown in the dashed box. The purpose of these three steps is to transform the frequency domain data $X(k), k=0,1,\ldots,N-1,$ into time domain as $S(n), n=0,1,\ldots,NM-1,$ where $N$ is the sub-carriers’ number, and $M$ represents the interpolation factor of up-sampling. Finally, a cyclic prefix (CP) is added to each symbol which is converted to analog $s(t)$.

Assuming that the OFDM symbol’s effective period is $T$, let us consider the prototype definition of $s(t)$ without CP in Figure 1. If the first sub-carrier’s analog angular frequency is $\Omega_i$, then the transmitted time domain baseband complex signal can be expressed as

$$s(t) = A \sum_{k=0}^{N-1} X(k) \exp\left(jk\Omega_i t\right)$$

where $A$ represents the amplitude factor of each sub-carrier, $k$ is the sub-carrier’s index and $j$ is the imaginary unit, $j = \sqrt{-1}$. Let $s(t)$ be sampled at the frequency of the DAC as depicted in Figure 1, then we can obtain the expression of $S(n)$ by substituting $t = nT / NM$ into Equation 1, i.e.,

$$S(n) = A \sum_{k=0}^{N-1} X(k) \exp\left(\frac{2\pi kn}{NM}\right)$$

where $n = 0,1,\ldots,NM-1$. 

Figure 1. Structure of traditional OFDM transmitter.
As indicated in Equation (1) and (2), both the analog and digital OFDM signals are generated by summing a number of modulated sub-carriers together. The analog sub-carriers in Equation (1) are difficult to generate by analog devices, due to the fact that their phases are hard to control by analog devices and the corresponding costs are expensive. However, it is convenient to construct these digital sub-carriers by DDS modules. DDS is a frequency synthesis technique that employs digital data to generate sinusoidal signals of variable frequencies [11]. The advantages for DDS to generate sub-carriers rely on its convenience to control its frequency and initial phase. Therefore, according to Equation (2), the primary architecture of DDS-based OFDM transmitter is shown in Figure 2.

\[ X(n) = S(n) + \sum_{k=0}^{N-1} e^{j\omega_k n} S_k(n) \]

Figure 2. The primary DDS based architecture of OFDM transmitter.

From Figure 2, one can find that the DDS-based OFDM transmitter comprises of \( N \) branches, each of which contains a complex exponential DDS module and a complex multiplier, denoted by “\( \times \)”. The \( k \)th branch’s DDS module is used to output the complex sequence \( A e^{j\omega_k n} \), \( n=0,1,\ldots,NM-1 \), where \( \omega_k \) denotes the first sub-carrier’s digital angular frequency. We note that \( \omega_k=2\pi/NM \), thus the \( k \)th branch’s DDS outputs sequence \( A e^{j(k)\omega n} \), and \( S(n)=A \cdot X(k) \cdot e^{j(k)\omega n} \). The notation “\( \times \)” in Figure 2 stands for a complex adder, which can sum up all the branches’ outputs in one clock cycle if implemented on FPGA.

The complex exponential DDS module is implemented by combining two conventional DDS modules together, with one module generating the real part and the other the imaginary part. More details of DDS principle can be found in [12,13], and the references therein.

Compared with the traditional IFFT-based OFDM transmitter, one of the advantages for the DDS-based architecture lies in that it has no latency between the time point when \( X(k) \) are ready and the time point when \( S(0) \) begins to be output. This relies on the fact that it is highly parallelized, i.e., each branch can generate a complex exponential signal in one clock cycle, and the adder can sum up all the branches’ data in a single clock cycle. Typically, the latency introduced by traditional IFFT-based structure between the same time points is dozens of microseconds, while for the DDS-based architecture, it is zero!

3 PROPOSED DDS-BASED ARCHITECTURE AND ITS SIMPLIFICATION

Although the primary DDS-based architecture has no latency compared with the traditional structure, it is still complicated. In this section, we aim at further optimizing its architecture by the following two aspects: making all the DDS modules share a communal memory bank and replacing all the multipliers by simple switches.

3.1 All DDS modules share a communal ROM bank

After closely inspecting the branches in Figure 2, one can find that all the digital angular frequencies of the DDS modules’ outputs are integer multiples of \( \omega_0 \). By exploiting this property, we are capable of designing a new structure, in which all the DDS modules share a communal ROM bank. Figure 3 demonstrates a schematic example for three traditional DDS modules that share a communal ROM bank and output their data sequences with respective digital angular frequencies of \( \omega_1=2\pi/24 \), \( \omega_2=2\pi/12 \), and \( \omega_3=2\pi/8 \).

![Figure 3. Schematic of three DDS modules sharing a communal ROM bank](image)

In this example, the communal ROM bank stores the data sequence \( A \cdot \sin(2\pi n/8) \), \( n=0,1,\ldots,23 \), and \( A \cdot \sin(2\pi n/24) \), \( n=0,1,\ldots,23 \), as depicted in Figure 3(a). To continuously output the sine sequence \( A \cdot \sin(2\pi n/24) \), \( n=0,1,\ldots,\infty \), we can repeatedly fetch the data from the ROM bank one by one per clock.
cycle. If we fetch one datum from every two data in the bank as described in Figure 3(b), i.e., repeatedly fetch the data with indexes 0, 2, 4, ..., 2k, and then the sine sequence \( A \sin(2\pi(2^n)/12), n=0,1,\ldots,\infty \) can be obtained. Similarly, by fetching one datum from every three, we can have the digital angular frequency \( 2\pi/3 \). Furthermore, to generate the data sequence with “\( \cos \)” format, such as \( \cos(2\pi(n)/12), n=0,1,\ldots,\infty \), it just needs to define that the first datum starts from the 6th index in Figure 3(a), which is equivalent to shifting 90° phase from the “\( \sin \)” sequence.

According to the proposed approach, if we use only one memory bank to store the sequence \( A \sin(n\omega)\), \( n=0,1,\ldots,\infty \), then the real part and imaginary part of each branch’s complex exponential sequence can be obtained as long as we fetch data at the interval of \( k-1 \). If expand the multiplication in Equation (2), and let \( X(k) = X_r(k) + jX_i(k) \), then

\[
S(n) = S_r(n) + jS_i(n)
\]

\[
= \sum_{k=0}^{N-1} [X_r(k)\cos(k\omega_0n) - X_i(k)\sin(k\omega_0n)] + j\sum_{k=0}^{N-1} [X_r(k)\sin(k\omega_0n) + X_i(k)\cos(k\omega_0n)].
\]

where \( S_r(n) \) and \( S_i(n) \) represent the real part and imaginary part of \( S(n) \) respectively. This equation implies that each complex multiplication can be implemented by four real multiplications. Accordingly, the architecture of OFDM transmitter can be simplified as shown in Figure 4. For ease of demonstration, we only depict \( S_r(n) \), since the quadrature part \( S_i(n) \) has nearly the same architecture.

In Figure 4, each branch contains two sub-branches and each sub-branch fetches a real data per clock cycle at its right interval from the communal ROM bank. The \( k \)th branch fetches data at interval of \( k-1 \), and the difference between sequence \( A \cos(k\omega_0n) \) and sequence \(-A \cos(k\omega_0n)\) relies on their initial phase from the ROM bank. The 0th branch’s digital angular frequency is 0, thereby its output becomes the constant \( A \).

Meanwhile, the multiple input single output (MISO) adder can sum up all the sub-branches’ data in one clock. This parallelism strategy empowers that the time domain data \( S_i(n), n=0,1,\ldots,\infty \), can be output one by one per clock cycle soon after the frequency domain data has been input to system.

### 3.2 Replace Multipliers with Switches

In this subsection, we will replace the multipliers in Figure 4 with switches to further simplify system structure. Obviously, except for the 0th branch, each branch contains two sub-branches. We note that each sub-branch has a multiplier to multiply the frequency domain data \( X_r(k) \) (or \( X_i(k) \)) by the DDS modules’ output data \(-A \sin(k\omega_0n)\) (or \(-A \cos(k\omega_0n)\)) per clock cycle. Usually, \( X_r(k) \) and \( X_i(k) \) belong to the same set with finite elements. For convenience, we denote the set as “modulation set”. For example, in the quadrature phase shift keying (QPSK) modulation, \( X_r(k) \) and \( X_i(k) \) belong to \{1,-1\}; in the 16 quadrature amplitude modulation (16QAM), the modulation set is \{3,-1,-3\}. Inspired by the shared memory bank in Figure 4, if the modulation scheme is fixed, then the two data input to each multiplier belongs to their respective set, therefore we can pre-calculate these results and store them in ROM banks. Finally, multipliers can be replaced by switches which are used to fetch data from the corresponding ROM bank at right decimation ratio. The two sub-branches in the \( k \)th branch fetch data at the decimation ration of \( k \).

![Figure 5. Simplified architecture of OFDM transmitter’s in-phase part \( S_r(n) \) by replacing multipliers with switches. (Note: the quadrature part \( S_i(n) \) has been omitted due to its similarity).](image-url)

Taking 16QAM as an example, we use two ROM banks with the first storing the sequence \( A \sin(n\omega_0n) \), and the second storing data \( 3A \sin(n\omega_0n) \), where \( n=0,1,\ldots,\infty \). Assuming that \( X_r(k)=3 \) and \( X_i(k)=1 \) are the input of the \( k \)th branch as shown in Figure 4, then the first multiplier is used to compute \( 3A \cos(k\omega_0n) \), and the second computes \(-A \sin(k\omega_0n)\).
It is found that the first multiplier’s products are stored in the second ROM bank if only we fetch the first data with the index $\frac{NM}{4}$, and then fetch other data from the same ROM bank at the decimation ratio of $k$ per clock cycle. Similarly, the second multiplier’s outputs are stored in the first ROM bank if only we fetch the first data from the $\frac{NM}{2}$-th element. By doing so, all the multipliers can be replaced with simple switches which only realize the function of “fetching data”. By combining the aforementioned two simplification methods, the proposed architecture of $S_i(n)$ is presented in Figure 5.

In Figure 5, each sub-branch uses a switch to replace its multiplier depicted in Figure 4. Data is fetched from one of the $r$ memory banks per clock cycle, where $r$ is equal to the number of different absolute values of the elements in the modulation set. For the lower order QAM modulation, $r$ is usually very small, such as $r=1$ for QPSK (the same as 4QAM) and $r=2$ for 16QAM. Assume that the modulation scheme of the OFDM transmitter is $x$-QAM, where $x$ is an integer power of 4, then

$$r = \sqrt{x}$$

(4)

Each ROM bank stores $NM$ data and these absolute values of the elements in the modulation set equal to $2m-1$, where $m=1,2,\ldots,r$, thus, the data sequence stored in the $m$th memory bank is expressed as

$$(2m-1) \cdot A \cdot \sin(\omega n),n = 0,1,\ldots,NM-1$$

(5)

By combining the foregoing two modifications, if the proposed architecture is implemented on FPGA, then its principle can be introduced as follows. When the OFDM transmitter starts working, the system clock generator begins to generate clock ticks. Then, at every positive edge of the clock tick, each switch fetches a datum from a ROM bank with the right initial phase. If the switch is in the $i$th branch, it should fetch all the subsequent data at the decimation ratio of $k$. If one sub-branch is going to fetch the data with the index (denoted as $y$) over $NM-1$, then the sub-branch should perform a modulo $NM$ operation, i.e., the next data index is $y$-$NM$. By this modulo method, each branch’s output data confirms to the expression in Equation (2), which can effectively eliminate the spurious [13] signals, since the proposed architecture does not really realize a single sinusoidal signal, and it can be summarized as a simple realization method of Equation (2).

These initial phases are $0^\circ, 90^\circ, 180^\circ$ or $270^\circ$, which are related to fetching the first datum with index $0, NM/4, NM/2$ or $3NM/4$ respectively. Let

$$d_k(n) = \pm |X_y(k)| \cdot A \cdot f(\omega n)$$

(6)

be the expression of these data fetched by the switch located in a sub-branch of the $k$th branch, where $X_y(k)$ represents $X_i(k)$ or $X_o(k)$, and $f(\cdot)$ stands for $\sin(\cdot)$ or $\cos(\cdot)$. The ROM bank number is determined by $|X_y(k)|$ according to Equation (5). If $|X_y(k)|=2m-1$, then the ROM bank number is $m$. The initial phase depends on Equation (5)’s sign being positive or negative and $f(\cdot)$ being $\sin(\cdot)$ or $\cos(\cdot)$. In general, there are four cases for these initial phases as shown in Table 1.

Table 1. The initial phases related to the data expressions

<table>
<thead>
<tr>
<th>$d_k(n)$ cases</th>
<th>$+\sin(\cdot)$</th>
<th>$+\cos(\cdot)$</th>
<th>$-\sin(\cdot)$</th>
<th>$-\cos(\cdot)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial phase</td>
<td>0°</td>
<td>90°</td>
<td>180°</td>
<td>270°</td>
</tr>
<tr>
<td>First index</td>
<td>$\frac{NM}{4}$</td>
<td>$\frac{NM}{2}$</td>
<td>$\frac{3NM}{4}$</td>
<td>$\frac{3NM}{2}$</td>
</tr>
</tbody>
</table>

For example, if one sub-branch intends to output $|X_y(k)| \cdot A \cdot \sin(\omega n), n = 0,1,\ldots,NM-1$, then its sign is negative, and it has the format “$-\sin(\cdot)$”. As a result, its initial phase is $180^\circ$, and according to Table 1, the first datum should be fetch form the $\frac{3NM}{2}$-th element of the ROM.

4 HARDWARE EXPERIMENTS ON FPGA

In order to investigate the performance of the proposed architecture, we conduct hardware experiments on Altera FPGA platform DE2 [14]. The OFDM system framework is based on the IEEE 802.11a standard. For comparison, two representative IFFT algorithms are employed. The first one is implemented by Quartus II Megacore, while the other one is realized by Mahdavi’s algorithm [15].

According to the IEEE 802.11a standard, the OFDM baseband signals contain 64 sub-carriers, thus, the IFFT transform length is 64. According to Figure 4 and Figure 5, we can conclude that for the proposed DDS-based architecture, 64 branches and 253 switches are exploited. For our hardware tests, we use 16QAM as the modulation scheme. From Equation (4), we can derive that $r = 2$, which means that the proposed architecture only employs two ROM banks. Assuming that the interpolation factor is $M = 4$, then the data sequences stored in the two ROM banks are $A \cdot \sin(2\pi n/256)$ and $3A \cdot \sin(2\pi n/256)$ respectively, where $n=0,1,\ldots,255$. Overall, the hardware complexity of the traditional OFDM transmitter contains a 64-point IFFT module, an up-sampling module and a LPSF (we use 41 taps), while in our DDS-based architecture the complexity relies on two ROM banks, 253 switches and two MISO adders.

In this section, we mainly compare the hardware consumption (HC), speed, and latency. Among them, HC is measured by total logic elements (TLEs) and embedded multipliers (Mults). Speed is measured using available maximum frequency (Max Freq), while latency refers to the clock cycles consumed by
the data transformation to output $S(0)$. All these experimental results can be observed from the development software. The platform uses Cyclone II EP2C35 FPGA chip with 483840 memory bits and 33216 logic elements (LEs). Via this information as well as the amount of consumed resource, the corresponding hardware consumption ratios and the performance comparisons are given in Table 2.

Obviously, the experimental data in Table 2 demonstrate that our proposed OFDM transmitter occupies less hardware resources compared with the traditional IFFT-based architecture, whereas it enables higher operation speed and lower latency. This is due to the fact that the proposed architecture does not need any multiplier and has much simpler control logic than the traditional architecture. Particularly, our proposed OFDM transmitter has zero latency during the transformation to output the first time domain data. This relies on the high parallelism of the system, i.e., each sub-branch can fetch a datum in one clock cycle, and meanwhile the MISO adders can sum up all these data.

**Table 2. Performance comparisons of the experiment.**

<table>
<thead>
<tr>
<th>OFDM Transmitter Method</th>
<th>IFFT by Megacore</th>
<th>IFFT by Mahdavi</th>
<th>DDS Based</th>
</tr>
</thead>
<tbody>
<tr>
<td>LEs</td>
<td>1090</td>
<td>930</td>
<td></td>
</tr>
<tr>
<td>IFFT Usage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mem/bits</td>
<td>14877</td>
<td>12700</td>
<td></td>
</tr>
<tr>
<td>CLKs</td>
<td>206</td>
<td>114</td>
<td></td>
</tr>
<tr>
<td>Total LEs</td>
<td>1362</td>
<td>1163</td>
<td>632</td>
</tr>
<tr>
<td>Total HCAnd</td>
<td>54</td>
<td>46</td>
<td>0</td>
</tr>
<tr>
<td>Mem/bits</td>
<td>19837</td>
<td>16934</td>
<td>9193</td>
</tr>
<tr>
<td>Latency</td>
<td>228</td>
<td>136</td>
<td>0</td>
</tr>
<tr>
<td>Total HC Ratio</td>
<td>4.1%</td>
<td>3.5%</td>
<td>1.9%</td>
</tr>
<tr>
<td>Max Freq/MHz</td>
<td>115</td>
<td>125</td>
<td>200</td>
</tr>
</tbody>
</table>

To quantify the hardware saving by the proposed architecture against the traditional architecture, we complementally implemented several OFDM transmitters with different sub-carrier numbers, and plotted the hardware resource consumption as a function of sub-carrier number in Figure 6.

Figure 6 demonstrates that the proposed DDS-based OFDM transmitter can save more than half of the hardware resource relative to that consumed by Megacore IFFT based architecture, and save almost half of the hardware resource compared to that consumed by Mahdavi’s IFFT-based architecture. It is also shown that the DDS-based architecture uses twice the hardware resource when the sub-carrier number doubles, whereas the IFFT-based architecture consumes more than the twice.

5 ORTHOGONALITY AND SPECTRUM ANALYSIS

The proposed architecture can be summarized as a simplification of Equation (2), which is derived from Equation (1) by sampling at the frequency of DAC. Therefore, the proposed architecture has the same characteristics as that in Equation (1). Moreover, since Equation (1) is the prototype definition of OFDM signal, it is evident that the digital signal generated by Equation (2) conforms to the definition of OFDM. To prove the orthogonality of sub-carriers in Equation 2, we can define $f(2\pi k_1 n/N)M$ and $g(2\pi k_2 n/N)M$ to be the subtracted in phase or quadrature part, and perform the following calculation

$$
\sum_{n=0}^{NM-1} f\left(\frac{2\pi k_1 n}{NM}\right) g\left(\frac{2\pi k_2 n}{NM}\right)
$$

where “f( )” and “g( )” stand for the arithmetic operation “sin( )” or “cos( )”. We observe that if and only if $f=g$ and $k_1=k_2$, Equation (7) is nonzero. As a result, we conclude that the digital sub-carriers generated by Equation (2), i.e., by the DDS-based method, are orthogonal.

Figure 7. The spectrum of OFDM transmitter: (a) the IFFT-based OFDM transmitter and (b) the proposed DDS-based OFDM transmitter.

In the IFFT-based OFDM transmitter, the frequency domain data is transformed into time domain by IFFT module, and then the time domain data is interpolated by an integer factor of $M$. In this procedure, its base band spectrum is repeated $M$ times as shown in Figure 7(a), where we set $M=2$ for instance. As a result, the
LPSF must be used to remove the redundant image spectrum which is shown in the dotted box in Figure 7(a). In contrast, for the DDS-based OFDM transmitter, Equation (2) demonstrates that its spectrum only contains the base band part as shown in Figure 7(b), i.e., has no image spectrum. Therefore, for the DDS-based OFDM transmitter, if we want to obtain the baseband spectrum, LPSF is indispensable. Furthermore, strictly suppressing the DDS-based spectrum in a certain bandwidth is possible. We can add a low pass filter (LPF) after the proposed architecture to filter out all the sidelobe outside the bandwidth. In the sense of this case, the LPF in the proposed architecture can focus its ability to filter out all the sidelobe, without the requirement to filter out the image as that done by the IFFT-based structure.

To fully understand the relationship between the proposed DDS-based method and the traditional IFFT-based method, observe these time domain data whose indexes are integer multiple of $M$ in Equation (2), i.e., $n = mM$, $m = 0, 1, ..., N - 1$, and substitute it into Equation (2), then

$$S(mM) = A \cdot \sum_{k=0}^{N-1} X(k) \exp \left( \frac{j 2\pi kmM}{NM} \right)$$

$$= A \cdot \sum_{k=0}^{N-1} X(k) \exp \left( \frac{j 2\pi km}{N} \right)$$

$$= A \cdot x(m), m = 0, 1, ..., N - 1,$$

where $x(m)$ is the IFFT of $X(k)$. We remark that, the time domain signal generated by Equation (2) is analogous to be interpolated from $X(k)$ by the factor of $M$. In other words, the DDS-based method directly interpolate $x(m)$ into time domain by the factor $M$.

6 CONCLUSIONS

In this paper, we mainly focused on improving the traditional IFFT-based OFDM transmitter, in terms of hardware consumption, latency, achievable maximum frequency, and the arbitrary transform length. A novel DDS-based OFDM transmitter has been presented. By making use of DDS signal’s two distinctive properties, we have proposed two further optimizations. The first one has made all the DDS modules share a small number of ROM banks so as to save memory consumption; while the second one has replaced all the multipliers with switches, which enables high operating speed. The advantage lies in that the proposed OFDM transmitter can avoid using IFFT, LPSF and multipliers, and has zero latency during the transform of obtaining the first time domain data from the frequency domain. Compared with the traditional OFDM transmitter, the proposed DDS-based architecture has saved hardware resources by more than 50%, and the available maximum frequency has outperformed the IFFT-based structure by more than 60%.

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