INTRODUCTION

RF Power Amplifiers (PA) is used in a wide variety of applications including wireless communication, Bluetooth, and Radar and so on. It is one of the most active research areas and has the largest power consumption in RF front-end. As one of the most challenging building blocks in the radio frequency (RF) transceiver chip, the performance of a PA is largely characterized by its power efficiency and linearity. Up to now, several techniques have been proposed for low power and efficient PA. The switch PA (class-D/E/F) is more popular than the linear PA (class-A/B/C/AB) because of their lower power consumption and larger conversion efficiency. However, high-performance inverter-based class-D RF amplifiers require fast p-devices, which demand higher standards of CMOS process [1-2]. The switched class-E has an ideal efficiency of 100 %, but the maximum theoretical peak voltage is about 3.67 times the supply, which calls for higher capacity withstand voltage of transistor, it is a major drawback [3-4]. The class-F PA achieves a high efficiency by uses a transmission line at the drain and a high-Q tank in parallel with the load resistor [3], however, several resonators with a high-Q are needed, requiring additional area, and the transmission line also cannot be directly integrated. Additional methods or architectures are used in switched amplifiers for amplitude modulation and linearization, such as out-phasing and LINC [5], supply modulation using polar transmitters [6], and pulse-width modulation [7-8] so on. The current-reused design [9-10] is an effective topology which can provide a desirable gain, because the transistors share the same DC current, the power consumption of the circuit can be reduced. The most common way to extend the tolerable supply voltage using low-voltage CMOS technology is to use the cascode or stacked transistor structure [11-12], which in combination with thick-oxide transistors allows devices to operate in higher supply voltage, and keeping a high level reliability at the same time. Besides, by using self-biasing and forward-body-bias technique [13-15], devices can give larger design space for voltage swing, reliability, and performance in the same or lower supply voltage. All of the methods or architectures we adopted are for the higher output power, higher load, and lower current, which potentially lead to lower losses and higher efficiency.

A Fully-integrated Highly Efficient CMOS Class-E Power Amplifier Using Cascode Class-E Drivers for WLAN Applications

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ABSTRACT: This paper presents a modified class-E single-ended power amplifier (PA) for WLAN application. The proposed class-E PA consisting of two stages, all driver stages adopts bias voltage technique to simplify the structure and improves RF performance. The driver stage adopts the forward body bias technique to lower threshold voltage and realize high efficiency with low operation voltage; the power stage utilizes cascode topology with a self-biasing voltage technique to reduce device stress. The proposed PA is simulated by cadence IC in TSMC 0.18-µm CMOS technology. With a 2.3 V supply voltage, the fully integrated CMOS PA achieves maximum output power of 27.8 dBm and power-added efficiency (PAE) of 48.3% at 2.4GHz. It achieves high power gain of 31.5 dB and large output power with low input signal. The chip area of the proposed class-E PA is 0.90 mm².

Keywords: class-E; CMOS PA; low power; forward-body-bias; WLAN

1 INTRODUCTION

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2 CIRCUIT DESIGN AND ANALYSIS

2.1 The basic class-E power amplifier

The class-E PA employs a single transistor operated as a switch. The drain voltage waveform is the result of the sum of the DC voltage and the drain voltage, when the RF signal charging the parallel drain-shunt capacitance and transistor internal capacitance, there is a corresponding voltage in the drain of transistor [11]. In optimum class-E, there is no overlap between the drain voltage and drain current waveform. When the transistor turns on, the drain voltage drops to zero and has zero slopes; when the transistor turns off, the drain current drops to zero and has zero slopes, so we can eliminate the switching losses and show a good tolerance of component variation [12]. Figure 1 shows the topology of a basic class-E PA. The element parameters design values [17-18] of classic class-E PA are show in Table 1.

![Figure 1. The schematic of basic class-E.](image)

Table 1. The element parameters design values of classic class-E PA.

<table>
<thead>
<tr>
<th>Element</th>
<th>Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shunt capacitor</td>
<td>( C_0 = \frac{P_0}{\pi \omega V_{DC}} )</td>
</tr>
<tr>
<td>Load impedance</td>
<td>( R_L = B V_{DC}^2 / P_0 (\pi^2 + 4) )</td>
</tr>
<tr>
<td>Resonant inductor</td>
<td>( L = 8 Q_0 V_{DC} / \omega P_0 (\pi^2 + 4) )</td>
</tr>
<tr>
<td>Resonant capacitor</td>
<td>( C = P_0 (\pi^2 + 4) / 8 \omega Q_0 V_{DC}^2 )</td>
</tr>
<tr>
<td>The remaining reactance</td>
<td>( X = \pi V_{DC}^2 (\pi^2 - 4) / 2 \omega P_0 (\pi^2 + 4) )</td>
</tr>
</tbody>
</table>

2.2 The proposed class-E power amplifier

Figure 2 shows schematic of the proposed class-E power amplifier. The designed PA adopts two level stages to reduce the high requirement of the input signal, which consist of driver stage and power stage. For the second level, the greater the continuity signal, the smaller the on resistance and power loss, if the driver stage can provide larger amplitude input signal to the power stage, it is useful to enhance the overall efficiency of PA. If the input sine signal is converted into square wave signal to drive the second stage, long conversion time from one state to another state in switching transistor could be avoid. So the class-E amplifier, class-F amplifier and inverter can be used as the driver stage.

2.3 The driver stage

Low supply voltage has brought great challenges to the analog integrated circuit design; one of the most important problems is that the analog signal dynamic range will decrease. There are two ways to solve this problem: changing the process or using useful circuit design technique.

The threshold voltage decides the smallest operating voltage, while the main factor influencing the threshold voltage is the source substrate bias voltage (\(V_{BS}\)); the important way to alleviate the threshold voltage limitation is add positive bias voltage to substrate of MOSFET. For NMOS and PMOS devices, the threshold voltage is divided as follows [9]:

\[
V_{thn} = V_{th0} + r \left( \sqrt{2 |\Phi_F| - V_{BS}} - \sqrt{2 |\Phi_F|} \right)
\]

\[
V_{thp} = V_{th0} - r \left( \sqrt{2 |\Phi_F| + V_{BS}} - \sqrt{2 |\Phi_F|} \right)
\]

\(V_{TH0}\) is the threshold voltage of MOSFET when \(V_{BS}=0\); \(r\) is body effect coefficient; \(\Phi_F\) is semiconduc-

![Figure 2. The schematic of the proposed class-E PA.](image)

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tor parameter, typical value is 0.3-0.4V [10]. When put a positive bias voltage in MOS substrate, the increasing \(V_{BS}\) lead to decrease of the threshold voltage. The working voltage of the whole circuit needs to meet the minimum requirements \(V_{DD} > nV_{TH}[10]\); \(n\) is the number of stacked layers. So \(V_{DD}\) is also reduced with the increase of substrate bias voltage.

Figure 3 shows the basic unit of driver stage. Figure 4 shows the relationship between the substrate leakage current and the equivalent threshold voltage changes with \(V_{BS}\) in MOSFET. In Figure 4, When \(V_{BS} > 0.5\), the leakage substrate current will rapid growth, this will make the whole circuit difficult to guarantee the stability of the PA. However, when the threshold voltage is too low even close to zero, the circuit is not in the cut-off region and devices working in weak inversion region, there will still be small current, the loss must be considered. So we are keeping the substrate bias voltage at around 0.4V.

\[
R_{ON} = \frac{1}{\mu_0 C_{GS}} \frac{W}{L} (V'_{GS} - V_{TH})
\]

\[
P_{out} = 0.557 \left(\frac{V'_{DD}}{V_{DD}}\right)^2\frac{1}{R_{load}}
\]

\[
V'_{DD} = V_{DD} - V'_{RON} P_{Loss} = i_d^2 (r_{DS1} + r_{DS2})
\]

\(V'_{DD}\) is effective supply voltage; \(r_{DS1}\) and \(r_{DS2}\) are the on resistance of M1 and M2 respectively. In the equation (3~5), we can know that the on resistance of transistor will be reduced with the decreasing \(V_{TH}\), which is resulting in the decreasing power loss and improving efficiency.

The power stage adopts a current mirror gate bias topology and forward-body-bias technique for better performance and higher output voltage. To alleviate the threshold voltage limitation of the transistor, positive bias voltage \(V_{bh1}, V_{bh2}\) is injected to the body of the transistor M1 and M3, larger resistance \((R_{bh1}, R_{bh2})\) added to stabilize current. The series LC network (L1, C1) serves as input matching network. A class-E pre-drive structure is consisted of transistor \(M1, M2, M3\) and \(M4\) and series LC network \((L3, C2, L4)\) are used to realize class-E operation and inter-stage matching network, \(L_{di}\) and \(L_{do}\) are isolate induct preventing the DC current directly leak to ground. The operation voltage \((V_{dd1})\) is from 1.0V to 1.5 V.

We use simulation tool Cadence to accomplish the input matching. The small signal mode of input impedance matching is shown in Figure 5.

\[
Z_{in} = \frac{g_m}{g_s} \frac{(W/L)}{j}\n\]

For simplicity, we can ignore miller effect; all other parasitic, transistor internal resistance and body effects are ignored. Where \(g_m\) is given by (6), their input impedance \(Z_{in}\) can be calculated in (7).

\[
\frac{1}{Z_{in}} = \frac{1}{SL_{b2}} + \frac{1}{R2} + g_{s2} + S(C_{gs1} + C_{ps2}) + \frac{1}{SC_{2} + Z_{s2}}
\]

When the C2 is a big capacitance, we can ignore the influence of \(Z_{s2}\); so the input impedance \(Z_{in}\) could be simplify as (8), it’s a function mainly related with transconductance \(g_{m2}\), \(L_b\) and \(C_{2}\). Therefore we can adjust the values of \(Z_{in}\) to acquire appropriate input matching, blocking the unwanted harmonic components and getting the max effective power.
\[ Z_{in} = \frac{1}{\frac{1}{S_{L6}} + \frac{1}{R2} + g_{m2}} \]  

(8)

2.4 The power stage

Figure 6 shows the big signal model scheme of power stage. The power stage adopts the cascode topology with inserted inductor (L5) on drain node of the common-gate transistor (M5). The self-biasing technique is mainly realized by R3 and C4, which is employed to reduce the peak voltage between drain and gate of M5. It makes the gate voltage of M5 change with the drain voltage of M5. Adjusting resistor R3 and capacitor C4, the drain-gate peak voltage of M5 and M6, we can make it the same, and then they can use the same dimensions.

Now, we will discuss the power losses of power stage.

When the switch is turn off, the switch transistor M5 and M6 are all operating in the linear region, the power losses in the nonlinear resistor of M5 and M6 is \( P_{\text{Loss}} \), which has an effect on the whole PA’s efficiency. We can calculate the power losses by (8):

\[ P_{\text{Loss}} = i_{ds}^2 (r_{DS} + r_{	ext{mode}}) \]  

(9)

When the transistor M5 and M6 are all operating in the cut-off region, current only flowing through the parasitic capacitance \( C_{DBS} \), the power losses is small and can be ignored.

When the switch transistor M5 is operating in the linear region and M6 is operating in the cut-off region, we inserted the inductor \( L_g \) on drain node of transistor M6 to eliminate influence of parasitic capacitance, which can rapidly improve the source voltage and shorten the charging time, reducing power consumption. The inductor \( L_g \) inserted on drain node of transistor M6 is used tuning out the parasitic capacitor \( C_{\text{block}} \) at the desired frequency of operation.

3 SIMULATION RESULTS

The proposed class-E PA has been fabricated in a standard 0.18-μm CMOS technology. Figure 7 shows the simulated waveform of drain voltage and drain current of M5. Where, \( V_{dd1}, V_{dd2}, V_{BS} \) and input power are 1.0 V, 2.3 V, 0.45 V and -5 dBm, respectively. In Figure 7, the current is almost zero and the voltage is non-zero when the transistor is at ON state; on the other hand, when the transistor is at OFF state, the current is non-zero due to the parasitic capacitance. The voltage and current are not maximum level at the same time, therefore, the power dissipation and the product of drain voltage and current are minimized and high efficiency can be obtained. The simulated output power and power gain at 2.4 GHz are shown in Figure 8. Where, the bias voltage, \( V_{dd1} \) and \( V_{dd2} \) and \( V_{BS} \) are 1.0 V, 2.3 V, 0.45 V, respectively. It can be seen that the proposed PA delivers the maximum output power of 27.8 dBm. Figure 9 shows Simulated S-parameters, the power gain is about 31.5dB. Figure 10 shows the simulated Pout and PAE versus supply voltage (\( V_{dd2} \)) with a fixed input power of -5 dBm. It can be seen that the increment of Pout is connected with the \( V_{dd2} \) when the supply voltage is swept from 1.5 V to 2.5 V. On the other hand, PAE is saturated when \( V_{dd2} \) increases to 2.3 V, its 48.3 % PAE. Figure 11 shows the layout of the proposed class-E PA.

Figure 7. Simulated time domain signal of drain voltage and drain current of M5.

Figure 8. Simulated output power (Pout) and Gain vs input power (Pin).
Table 2 presents the comparison of performances of the reported CMOS class-E PAs. From Table 2, the proposed class-E PA can obtain higher efficiency, higher power gain in same operate frequency compared with these PAs proposed in the previously papers.

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