A High Voltage Low Ripple Voltage Multiplier Circuit and Its Characteristics Analyses

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Abstract. The ripple voltage and voltage drop of Cockcroft-Walton voltage multiplying rectifiers are affected by the square or cube of stage number respectively. When increasing the number of the stage, the ripple voltage and voltage drop would significantly increase. For overcoming this problem, the proposed circuit adopts phase shift superposition to realize 2N time voltage multiplier circuit. By using three-phase transformer composed by three independently single phase transformer, output winding is connected to DC double voltage circuit. 12 times voltage circuit is built by parallel input, serial output to realize 6 pulses periodic superposition. Through the overlay, the ripple is greatly weakened. The theoretical analysis is made for ripple and voltage drop, and comparisons to the typical and symmetrical Cockcroft-Walton multistage voltage multiplier circuit are carried out. Results show that the circuit can significantly reduce the voltage ripple and voltage drop, and significantly shorten the output voltage steady set up time.

Introduction

The problem of voltage multiplying rectifier is ripple and large voltage drop, which increases with the number of the stages of voltage multiplier. When the input voltage, load and the average voltage are certain, the current ripple and voltage drop are respectively influenced by the square or cube of stage number [1-5]. In order to reduce the ripple and the voltage drop, this paper proposes a new voltage multiplying rectifier circuit. By using the three-phase transformer, the output voltage is the superposition of input voltage by phase-shift and oppose-phase, so realizing one 6th cycle phase shift. The voltage multiplying rectifier circuit not only reduces the ripple of multiple voltage circuit and voltage drop by phase shift superposition, but also by reducing the number of the stages, thus significantly reduces the ripple of the circuit. The circuit is particularly suitable for higher demand of low ripple output voltage and low voltage drop.

The Characteristics and Scheme of Circuit

The traditional voltage multiplying rectifier generally takes the circuit as Cockcroft-Walton voltage multiplier (CWVM). We assume that the output current is \(I\), and the number of the stage of multiplier is \(N\), and the capacity of each capacitor is the same, and the frequency of the AC power is \(f\), the voltage drop is as follows.

\[\Delta U_1 = \frac{(4N^3 + 3N^2 - N)I}{6fC}\] (1)

And the ripple voltage is as follows:

\[\Delta U_2 = \frac{(N + 1)NI}{4fC}\] (2)

So for the higher stage multiplier, the load capacity is low. Just only small output current or power can also lead the considerable voltage drop.
To make the ripple and voltage drop small, the stage number must be less. But when the input voltage is certain, the output voltage is accordingly low. In document [6-9], the circuit is improved based on symmetry type Cockcroft-Walton (SCWVM), the ripple are reduced to some extent, but the stage number is still high, therefore the ripple and voltage drop problem are not solved significantly. The proposed circuit uses the lowest stage double voltage circuit superposing to reduce the ripple and voltage drop. The scheme is as Fig.1, and the circuit structure is as follows: using three-phase transformer with individual iron core for each phase, then the output winding is connected to DC double voltage circuit.

![Figure 1. Proposed low ripple Cockcroft-Walton voltage multiplier circuit.](image)

**Circuit Analyses**

First we assume that the circuit is in stable state, and the load is purely resistor. In the circuit, the relationship of value of capacitor is as follows:  \( C_{2n} = C_2, C_{2n+1} = C_1 \) \( (n = 2,3,...,6) \). And the output voltage of A phase is \( U_m \sin \omega t \). So the wave shape across the capacitor \( C_2 \) is as Fig.2. Take the moment \( t_0 \) as start point of a cycle. At the time of \( t_0 \), the capacitor begin to be charged until time of \( t_1 \), then the capacitor discharges through the load until \( t_0 + T \). At the end of last cycle, the voltage value of capacitor \( C_1 \) has been charged to peak value \( U_m \). We assume that at the time of \( t_0 \), the voltage value of is \( u_{c2}(t_0) \), so we have

\[
U_m \sin \omega t = u_{c2(t_0)} + \frac{1}{C_2} \int_0^{t_1} i_{c2} \, dt + \frac{1}{C_1} \int_0^{t_0} (i_{c2} + I_R) \, dt - U_m \tag{3}
\]

And

\[
i_{c2}(t) = \frac{U_m \omega \cos \omega t - \frac{1}{C_1} I_R}{\frac{1}{C_1} + \frac{1}{C_2}} \tag{4}
\]

At \( t_1 \), the current through capacitor

\[
C_1: i_c1 = i_{c2} + I_R = 0 \tag{5}
\]

Where \( i_{c2}, I_R \) is the current through \( C_2 \) and the load.
Accordingly
\[ t_1 = \frac{1}{\omega} \arccos \left( I_R / C_2 U_m \omega \right) \] (6)

So the voltage across the \( C_2 \) is:
\[ u_{C2}(t) = \frac{C_2 U_m}{C_1 + C_2} \sin \omega t - \frac{I_R t}{C_1 + C_2} + u_{C2}(t_0) \quad t_0 < t \leq t_1 \] (7)

\[ u_{C2}(t) = u_{C2}(t_1) e^{\frac{t-t_1}{\tau}} \quad t_1 < t \leq t_0 + T \] (8)

Where \( \tau = \frac{1}{\sum_{k=1}^{6} \frac{1}{C_{2k}} } \). Because in stable state, the voltage across \( C_2 \) is the same at time of \( t_0 + T \) and \( t_0 \), therefore
\[ u_{C2}(t_1) e^{\frac{t_0 + T - t_1}{\tau}} = u_{C2}(t_0) \] (9)

At \( t_0 \), D1 conducts critically, therefore:
\[ u_{C2}(t_0) = U_m (1 + \sin \omega t_0) \] (10)

From equation (6) to (10), we have deduced the distribution of voltage across \( C_2 \). The other voltage cross \( C_{2n} \) lead or lag to the \( C_2 \) \( \frac{K T}{6} \) (\( K = 1, 2, \ldots, 5 \)). If we assume the voltage across \( C_2 \) is \( F(t) \), we can get the voltage across the load is:
\[ u_o(t) = \sum_{K=0}^{5} F(t - \frac{KT}{6}) \] (11)

We can easily know that the cycle period of the voltage across the load is \( \frac{T}{6} \). So we have:
\[ u_{O_{\text{max}}} = 6U_{C2m} + u_{C2}(t_1) \sum_{K=1}^{5} e^{\frac{t_1 - \frac{KT}{6}}{\tau}} \] (12)

\[ u_{O_{\text{min}}} = 6u_{C2}(t_1) + u_{C2}(t_1) \sum_{K=1}^{5} e^{\frac{t_1 + T - \frac{KT}{6}}{\tau}} \] (13)

The maximum voltage value across \( C_2 \) is
\[
U_{c2m} = \frac{C_m U_m}{C_1 + C_2} \sin(\arccos\left(\frac{I_R}{C_m U_m \omega}\right)) + u_{c2}(t_0) - \frac{I_R}{(C_1 + C_2) \omega} \arccos\left(\frac{I_R}{C_m U_m \omega}\right)
\]  
(14)

So the voltage drop and ripple of total output voltage are

\[
\delta_U = 12U_m - 6U_{c2m} - u_{c2}(t_1) \sum_{k=1}^{\frac{t_1 - KT}{\tau}} e^{\frac{-kT}{\tau}}
\]

\[
\Delta U = 6[U_{2max} - u_2(t_1)] + u_{c2}(t_1) \sum_{k=1}^{\frac{t_1 - KT}{\tau}} e^{\frac{-kT}{\tau}} (1 + e^{\frac{T}{\tau}})
\]  
(15)

We assume that at \( t_m \), the voltage value is at peak value, therefore:

\[
U_m + u_{c1} = u_{c2}(k)
\]  
(16)

In the mean time, the charging time to \( C_2 \) is short, so we can neglect the charge from \( C_1, C_2 \) to the load, so the variable of charge at \( C_1, C_2 \):

\[
\Delta Q = C_1(U_m - u_{c1}) = C_2(u_{c2}(k) - u_{c2}(k - 1))
\]  
(17)

Where \( u_{c2}(k) \) is the voltage value of \( C_2 \) after charging for \( k \) time, because the ripple is small relative to the mean voltage value, so \( u_{c2}(k) \) can be taken as voltage value after \( KT \) periods. So from equation (15) and (16), we have:

\[
u_{c2}(k) = 2U_m + \left(\frac{C_2}{C_1 + C_2}\right)^k (u_{c2}(0) - 2U_m)
\]  
(18)

Take the time when the ratio of transient voltage to steady-state voltage value being \( \gamma \) as characteristic time for establishing the steady sate, and that time is

\[
NT = \frac{\ln(2(1 - \gamma)) - \ln(2u_m - u_{c2}(0))}{\ln(C_2) - \ln(C_1 + C_2)} T
\]  
(19)

The Characteristics of the Circuit

Wave Shape Comparison

According to the proposed circuit scheme, the advanced multiplier is designed. For simplification, we make the secondary output voltage peak value is 300V, and the load resistance is 360kΩ, and all the capacitance values of the capacitor of the double voltage circuit is 100μ. Comparing the final output voltage wave shape of the proposed circuit to CWVM and SCWVM type circuit, we can have Fig.3. By the comparison of wave shape, we know that voltage drop for the proposed circuit is 18V, and the ripple voltage is only 3V, where as 300V, 40V for CWVM, and 176V, 20V for SCWVM. If we take value of the \( \gamma 0.999 \), the stable state establishing time is 0.2s, which is approximate the calculating value. whereas the stable state establishing time for CWVM and SCWVM is 5s. Therefore the performance of proposed circuit is greatly enhanced.

Circuit Load Characteristics

On the base of above design, we change the load circuit, and we can get the load characteristic as Fig.4. From the Fig.4, we know that for the proposed circuit, the ripple voltage and voltage drop are all small when load resistor change from 30kΩ to 360 kΩ. But for the CWVM and SCWVM circuit, the load characteristic became considerably poor when the load resistor is smaller than 100kΩ.
Conclusion

The proposed voltage multiplying rectifier takes the double circuit as basic block, and take advantage of the three phase transformer to input in parallel, and output in series. By superposition to reduce the ripple and improve the performance of load characteristic.

Figure 3. a The ripple voltage waveshape contrast with load of 360kΩ.
(From top to the bottom, the wave shapes are respectively corresponding to: Proposed low ripple voltage multiplier circuit, symmetry type SCWVM, typical CWVM)

Figure 3. The voltage wave shape contrast.

Figure 4. a The ripple voltage contrast with different load.

Figure 4. b The drop voltage contrast with different load.

Figure 4. The load characteristics contrast with different load.

From the analysis, we know that by the proposed circuit, in the case of certain input and output voltage, the number of multiplier stage can be reduced, therefore significantly reduce the ripple and voltage drop.
In this paper, the method of reducing the ripple voltage and voltage drop by the phase shift superposition makes very strong sense in practice. The proposed circuit has been applied for patent. But at the same time, the new circuit put forward higher requirements to the transformer insulation. For the circuit, there is a good application prospect in the case of large load power and require very low ripple.

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References


