The Design of a Portable Control Module Based on TMS320C6748 and FPGA

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Abstract. This paper proposes a portable control module based on TMS320C6748 and FPGA. We take advantage of the rich interface resources of TMS320C6748, including LCD/DDR2/Ethernet/EMIF/uPP etc. And we also use FPGA plus the PCI bridge chip, UART transceiver and CAN transceiver to realize the system control module. This control module includes interactive module, memory module and communication module. The control module has the characteristics of low power consumption, high reliability and low cost. It can replace the general-purpose CPU board in the field of portable test and meet the resources and performance requirements. So it has great application value.

Introduction

Currently many test devices in the outdoor portable testing field are based on "General-purpose CPU motherboard + Dedicated interface board + Dedicated interface adapter" architecture. This architecture is easy to upgrade or extend, but it also has large consumption, big size, high cost and complex system. For outdoor portable test equipment, it requires a simple interactive interface, adequate communication interface resources, small size and high reliability. But the requirement of the data computing ability and storage capacity requirements are not too high. The above general-purpose CPU architecture cannot meet the requirements well. So it is urgent to develop a new architecture.

TI's TMS320C6748 is an ultra-low-power fixed-point and floating-point DSP chip. Its build-in graphic library is user-friendly to realize the display of text, graphics or widget. Its unique power and sleep controller PSC can be used to reduce power consumption. It also has rich communication interface resources, including the commonly used communication interfaces [1] [2]. Simple compile environment SYS/BIOS or Starter Ware provide adequate resources of TMS320C6748 for user to quickly carry out the programming. In order to meet the interface resources, we add a FPGA chip mainly used to achieve CPCI bus. The control module based on the DSP + FPGA architecture can meet the requirements of portable testing device in resources and performance.

Demand Analysis

In order to meet the requirements of portable test device, the system is required to have the interaction module (display, audio, keyboard, mouse), the storage module (program memory and data memory) and the communication module (UART/USB/CPCI/Ethernet).

One kind general-purpose CPU motherboard used in test filed which meets these requirements above will be described next in the respect of its resources. The resources include interaction module: audio/VGA/LVDS, memory module: DDR3/Flash/SATA and communication module: USB/UART/Ethernet/CPCI/CAN. And we make a comparison between it and TMS320C6748 in Table 1.
Table 1. The comparison between general-purpose CPU motherboard and TMS320C6748.

<table>
<thead>
<tr>
<th></th>
<th>RAM</th>
<th>Flash</th>
<th>ATA</th>
<th>UART</th>
</tr>
</thead>
<tbody>
<tr>
<td>General-purpose CPU</td>
<td>DDR3 1066M</td>
<td>64M</td>
<td>6xSATA2.0</td>
<td>6x</td>
</tr>
<tr>
<td>C6748</td>
<td>DDR2 256M(max)</td>
<td></td>
<td>1xSATA2.0</td>
<td>3x</td>
</tr>
<tr>
<td>Ethernet</td>
<td>Display</td>
<td>USB</td>
<td>Audio</td>
<td>CPCI</td>
</tr>
<tr>
<td>10/100/1000</td>
<td>VGA/LVDS</td>
<td>1600×1200</td>
<td>4×2.0</td>
<td>Yes</td>
</tr>
<tr>
<td>10/100</td>
<td>LCD 1024×1024</td>
<td>1×1.1</td>
<td>1×2.0</td>
<td>McASP</td>
</tr>
</tbody>
</table>

From the table above, we can see TMS320C6748 meets most of the resources requirements. Though the Ethernet supports maximum speed to 100Mbps and the DDR2 supports maximum capacity to 256M, they both meet the requirements in the portable test field. When we make full use of TMS320C6748 interface resources, we also need to use a FPGA to achieve CPCI and CAN bus.

The Hardware Design of TMS320C6748+FPGA

The design part mainly includes the design of the power supply module, the interaction module (LVDS/VGA/Audio), the memory modules (Flash/SDRAM/SATA) and the communication module (USB/UART/CAN/Ethernet). Besides, the DSP and FPGA are connected by EMIF and uPP. Figure 1 shows the overall structure diagram:

The Power Supply Design

TMS320C6748 voltage supply needs the 1.3V, 1.2V, 1.8V and 3.3V. We select TI's TPS650250 to generate the corresponding voltage and make the FPGA to control the corresponding voltage output enable pins to control the power-on sequence to avoid the damage to the device. FPGA voltage is supplied by TPS70445's outputs 3.3V and 1.2V. At a temperature less than 25°, TPS650250 power consumption is 2.85W and TPS70445 consumes 4.115W. So the total consumption is 6.965W which is very low. Figure 2 shows the DSP and FPGA power supply scheme.

The Interaction Interfaces Design

The LVDS Interface and Touch Screen Control. TMS320C6748 contains an LCD controller that supports resolutions up to 1024 × 1024 with a total of 16 data lines. Since the LCD signals transfer in parallel mode, it brings the high signal voltage, the too much connection cables and the low anti-interference ability. In order to enhance the display reliability of the video signal, we
convert the LCD signal into LVDS signal. LVDS (Low Voltage Differential Signaling) signal is a kind of low voltage differential signal with very low voltage swing (about 350mV) [3]. This conversion reduces the noise and power consumption. We select conversion chip SN75LVDS83B. It can convert the digital RGB signals outputted by LCD into LVDS signals in 6/8 bit output mode without additional programming. Figure 3 is the design block diagram to convert LCD signal into LVDS.

To facilitate control, we will use a resistive touch screen. The resistive touch screen controller has a 4-wire or 5-wire mode. The 5-wire mode can get higher precision coordinate and longer lifetime than the 4-wire mode [4], so we choose the 5-wire mode touch screen controller. Here we select ADS7845 with ADC accuracy of 12 bits. TMS320C6748 connects the ADS7845 through the SPI interface to control and acquire the coordinate. Figure 4 shows the touch screen control scheme.

Figure 4. Touch screen control.  
Figure 5. Convert LCD signal into VGA.

The VGA Interface. Meanwhile, in order to deal with the device only has VGA interface, we add the conversion chip ADV7342 to convert LCD signal into VGA signal. ADV7342 supports the fast data transfer, so here we can use the TUSB2046’s USB 1.1 interface to realize this. Since there is only one USB 1.1 interface, we need to extend it through a USB hub. We choose TUSB2046B which can extend one USB port to four USB port without additional programming. The two remains are as spares. Figure 7 is a block diagram of the design. In order to achieve high reliability of power management, we take use of the power-on control pins PWRON and the overcurrent monitoring pins OVRCUR of the TUSB2046B. We also take use of the power-distribution switch TPS2044B’s overcurrent monitoring pins OC and enable pins EN. The TUSB2046B works in single control mode. When TPS2044B monitors the overcurrent condition, the OC pin will be pulled low, then the OC output will pull the TUSB2046B’s OVRCUR pin low. Thus the TUSB2046B’s PWREN outputs low voltage to pull the TPS2044B’s EN pin low to turn off the corresponding voltage output without affecting other ports. This module adds the USB port transient suppressor SN75240 to achieve ESD protection.

The USB Keyboard and Mouse Interfaces. This module needs the keyboard and mouse interfaces in order to facilitate the control and operation. The keyboard and mouse does not require fast data transfer, so here we can use the TMS320C6748’s USB 1.1 interface to realize this. Since there is only one USB 1.1 interface, we need to extend it through a USB hub. We choose TUSB2046B which can extend one USB port to four USB port without additional programming. And the two remains are as spares. Figure 7 is a block diagram of the design. In order to achieve high reliability of power management, we take use of the power-on control pins PWRON and the overcurrent monitoring pins OVRCUR of the TUSB2046B. We also take use of the power-distribution switch TPS2044B’s overcurrent monitoring pins OC and enable pins EN. The TUSB2046B works in single control mode. When TPS2044B monitors the overcurrent condition, the OC pin will be pulled low, then the OC output will pull the TUSB2046B’s OVRCUR pin low. Thus the TUSB2046B’s PWREN outputs low voltage to pull the TPS2044B’s EN pin low to turn off the corresponding voltage output without affecting other ports. This module adds the USB port transient suppressor SN75240 to achieve ESD protection.
The Memory Design

TMS320C6748 can be connected to an ordinary SDRAM via EMIF or connected to a DDR2 SDRAM via DDR2 interface. The DDR2 interface support storage up to 256MByte. In order to increase the speed of data exchange, we select the DDR2 SDRAM. The chip selected is K4T1G164Q1 with 64M x16 bit. The program memory expansion is realized by connecting a NOR Flash (W25Q32FV, 32Mbit) to TMS320C6748’s SPI port. TMS320C6748 also boot from this NOR Flash. In order to realize that the data can be stored when the power is off, we need connect a 128G SSD to TMS320C6748’s SATA interface which supports SATA2. For FPGA we connect a NOR Flash XCF32PVOG48C (32M) to FPGA for configuration of FPGA. Figure 8 shows the total storage solution.

![Figure 8. Storage solution.](image1.png)

The Communication Interfaces Design

The USB Interface Design. The module requires a USB interface for communication with the device with the USB interface. The USB 2.0 OTG interface of TMS320C6748 can be used. This USB 2.0 port supports high-speed and full-speed operation as a peripheral and supports high-speed, full-speed and low-speed operations as a host. It is used for high speed data transmission. To increase the reliability of the module, an ESD protection chip SN75240 is applied.

The Ethernet Port Design. TMS320C6748 contains an EMAC and a MDIO port. EMAC controls the data flow from the system to the PHY and MDIO controls of the configuration of PHY and the status detection. EMAC/MDIO can support 10/100Mbps Ethernet operation. EMAC has two interfaces Media Independent Interface (MII) and reduced MII (RMII). We choose the LAN8710A as the Ethernet transceiver and the MII transceiver lines and control lines are connected to the LAN8710A. Figure 9 shows the Ethernet port design.

The Serial Ports Design. UART is most widely used in system and transmits a variety of data. We can use TMS320C6748’ three UART, but their transmitter and receiver FIFO is only 16 bytes. The FIFO depth is too small, so the data transmission will be interrupted more frequently when receiving or transmitting a certain amount of data. The system transmission performance will be degraded. In order to achieve efficient and reliable data transmission, we choose the FPGA to extend the UART instead of the built-in DSP’s UART. We select two SP3232 chips to extend four RS232 ports and select two MAX3490 chips to extend two RS422 ports. The FPGA can be programmed to achieve adjustable channel, baud rate, parity bit, stop bit and FIFO depth of UART. So the use of UART is more flexible and convenient. In order to enhance the system reliability, we add the TLP2362 for optical isolation and add the SMDA12C for the RS232 ports ESD protection and the SMDA05C for RS422 ports ESD protection. Figure 10 shows the UART port design.

The CAN Bus Design. To meet with the communication with the device having the CAN bus, we connect the FPGA to a CAN controller and a CAN transceiver to realize the CAN bus. To
improve data transmission speed, we select the CAN controller SJA1000T with parallel port. The SJA1000T is a dual-channel transceiver and supports CAN2.0 with data transfer rates up to 1Mbits/s. The FPGA signal voltage is 3.3V and the CAN controller SJA1000T signal voltage is 5V while the CAN transceiver SN65HVD233 signal voltage is 3.3V, so we need the level-shifting transceiver for voltage translation. Figure 11 shows the CAN bus design.

The CPCI Bus Design. The CPCI bus is the communication bridge between the control module and the outside. The CPCI communication speed and reliability will influence the performance of the module directly, so the CPCI design is very important. The architecture based on “FPGA+ PCI bridge chip” is mature and reliable. We choose the PCI bridge chip PCI9656 and make it work under 32bit/66M, direct host mode and C mode without hot-swap and power management. Figure 12 shows the simplified CPCI bus design.

![Figure 12. The simplified CPCI bus design.](image)

The Communication Interface between DSP and FPGA. There is a large amount of data transmission between DSP and FPGA. DSP and FPGA have many connection methods. Here we connect them via TMS320C6748’s uPP and EMIF interfaces. uPP is a kind of high speed parallel interface and its data lines and extended data lines are both 16 [5]. It can achieve very high-speed data transmission between DSP and FPGA. But the uPP does not contain the address lines while the FPGA establishes many corresponding registers to control the peripherals. So it is inconvenient for DSP to operate the FPGA peripherals via uPP without address lines. In order to solve this problem we also connect the DSP to the FPGA via EMIF.

The maximum clock frequency of the uPP is 1/4 CPU clock frequency when the uPP works in single data rate mode. The CPU clock frequency is 456MHz, then the uPP clock frequency is 114MHz. From the uPP timing diagram, the data transfers once per uPP period. The data transfer rate is up to 228MBps when in 16-bit mode. The data transfer rate of the PCI9656 is 264MBps in 32bit/66M mode while the FPGA will not reduce the CPCI data transfer rate significantly. So the module CPCI performance will meet the requirements.

The Software Design

The software of TMS320C6748 is compiled under SYS/BIOS or StarterWare, both of which provide users with abundant library resources and a simple way to compile. This will greatly facilitates the user's development. To design the program of LCD display under StarterWare, for example:

StarterWare provides rich libraries for the TMS320C6748. The Graphics Library containing Canvas/Checkbox/Container/Button/Listbox/Slider provides great convenience to display text/pictures/widgets. Figure 13 is the LCD display and the touch control flow chart. The “LCD Init”
includes Clock/DMA/Mode/Parameter/FIFO/Delay etc. The “Touch Init” includes Coordinate Init /Touch Detection Setup/SPI Init.

Summary

Low power consumption, low cost and high reliability have been pursued in outdoor portable test filed all the time [6]. The control module based on the TMS320C6748 and FPGA proposed in this paper has the following advantages:

Low power consumption: the DSP and FPGA power consumptions are lower than 7W.

High reliability: the chips selected meet industry standards. The vulnerable devices such as UART and USB will be added the ESD protection, isolation or overcurrent detection. Besides, the LCD signal converted into LVDS signal and touch screen control using the 5-wire mode also enhance the module reliability.

Low cost: the master control chips costs are less than the general-purpose CPU. The heat is less, so the cooling device of the peripheral requires low and the cost will be reduced.

Abundant interface resources: USB/UART/Ethernet/CPCI/CAN/LCD/VGA etc.

Above all, the control module based on TMS320C6748 and FPGA has a certain value in portable test filed.

References