Optimization Strategy of Reduction of Switching Times in Rectifier Stage Based on Power Electronic Transformer

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Keywords: Power electronic transformer, Double closed-loop control, Quasi-PR controller, Harmonic characteristics.

Abstract. The control strategies of conventional power electronic transformer are mostly double closed-loop control based on dq coordinate decomposition, and the control strategy is complex. Based on the analysis of the topology of single phase cascaded power electronic transformer, this paper takes the transformer primary rectifier as the typical object. According to the multilevel synthesis strategy, an improved ladder wave level control strategy is proposed and the quasi-proportional resonance is proposed. The simulation results show that the new control strategy can verify the proposed scheme by ensuring that the total voltage of the rectifier stage is maintained at a given value, the voltage of each module rectified voltage is approximately equal, and the switching frequency of the switching device is greatly reduced, and power factor of grid approaches 1.

Introduction

Based on how many power conversion links, the circuit topology of power electronic transformers is generally divided into bipolar, three-level and four-level, because four-level structure (AC/DC and DC/AC) topology at the input stage and output stage containing DC links can facilitate all types of distributed power systems connect to the corresponding DC bus, which is more flexible, thus this article adopts this kind of topology. At present, the control method of the input high voltage level of power electronic transformer generally adopts carrier phase shifted PWM (CPSPWM), which can shift a certain number of signals through the inter-scaling module carrier at a relatively low switching frequency. Reference [2] uses carrier phase shifting control technique for the input stage rectifier of power electronic transformer, and finally ensures that the phase angles of phase shifts of N carriers constitute 0, $2\pi*1/n$, $2\pi*2/n$, $\cdots$, $2\pi*(n-1)/n$, and the number of levels is $(2n+1)$, which reduces the distortion rate, but each module works in high-frequency mode, the number of switch is large and losses cannot be ignored. The literature [3] adopts hybrid PWM (HPWM) method, only one module is operated in PWM mode in each period of time, and other modules work in the fundamental frequency mode, which greatly reduces the switching frequency, but the voltage-sharing strategy between modules use digital signal processor (DSP) and field programmable gate array (FPGA), the overall control strategy is complex and difficult.

Based on the hybrid pulse width modulation strategy, this paper analyzes the working principle and implementation method of the topology circuit, adopts the appropriate module work pattern matching, automatically realizes the voltage equalization between the cascaded modules, and improves the current control strategy in the conventional double closed-loop, a quasi-proportional resonance control is applied to realize the accordance of grid-side voltage phase and current phase, and the simulation results on the MATLAB platform show that the new control strategy can achieve unity power factor operation at the grid-side and reduce the switching frequency of the power device.
Topology and Control Strategy of Cascaded PET

Topology of Cascaded PET

The cascaded topology consisting of IGBT full-bridge modules is shown in figure 1. It is divided into three stages: cascaded H-bridge (CHB) and isolated bidirectional full-bridge dc-dc converter (IBDC), output level. The grid-side AC power is converted to DC by the input stage. The transformer's primary inverter stage uses a 50% duty cycle modulation to convert the DC power to high-frequency AC power. The high frequency high voltage AC power is converted to high frequency low voltage AC power through a high frequency transformer. In the topology shown in figure 1, the primary L of transformer represents the filter inductance, \( u_s \) represents the AC voltage supplied from the grid terminal, and the capacitor C of the rectifier stage represents the filter capacitor, which is cascaded with n modules, \( u_{dci} \) represents the DC side voltage of the ith module, the ratio of high frequency transformer is n:1, and the current \( i_s \) represents the current of the grid bus.

![Figure 1. Cascaded power electronic transformer topology.](image)

Control Strategy of Input Rectifier Stage

From the circuit topology of figure 1, it can be described by KCL and KVL theorem:

\[
\begin{align*}
    u_{aa} &= \sum_{i=1}^{n} u_i \\
    u_s &= L \frac{di}{dt} + u_{aa} \\
    u_i &= s_i u_{dci}
\end{align*}
\]

where \( s_i \) represents the switching function of the ith H-bridge, and

\[
    u_i = \begin{cases} 
    u_{dci}, & (s_i = 1) \\
    0, & (s_i = 0) \\
    -u_{dci}, & (s_i = -1)
    \end{cases}
\]

![Figure 2. Hybrid PWM method.](image)
Figure 2 shows the comparison between the multilevel voltage $u_{an}$ synthesized by the three modules and the reference voltage signal of the voltage outer loop when the original square rectifier stage of the power electronic transformer adopts the hybrid pulse width modulation method under the three module cascaded mode. The working process can be seen as follows: the reference voltage enters the modulation link, and the reference voltage is:

$$u_r = U_m \sin(w \cdot t + \theta)$$  \hspace{1cm} (3)

Then determine which section the current reference voltage is, the basis for the judgment is:

$$k = \text{fix} \left( \frac{u_r}{u_{dc}} \right) + 1$$  \hspace{1cm} (4)

$\text{fix}(x)$ is represented in MATLAB by rounding to zero. At this time, $(k-1)$ modules of $n$ submodules can operate in the fundamental frequency switching mode, and only one module can work in high frequency PWM mode, the remaining $(n-k)$ modules work in zero state mode.

**Status Schedule and Control Strategy of Hybrid Pulse Width Modulation**

**Status Schedule Selection**

According to the above analysis, only one submodule works in PWM mode within each time segment. To ensure that the DC voltage is maintained near a given reference value, it is necessary to reasonably allocate the working mode of each module in the cycle, there are three main modes after analysis:

| Table 1. Three sorting tables of hybrid pulse width modulation algorithm |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| (a) Submodule 1 assumes all PWM task. |
| M1  | P | P | P | P | P | P | P | P | P | P | P |
| M2  | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | -1 | -1 | 0 | 0 |
| M3  | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | -1 | -1 | -1 | 0 |
| t   | t0~t1 | t1~t2 | t2~t3 | t3~t4 | t4~t5 | t5~t6 | t6~t7 | t7~t8 | t8~t9 | t9~t10 |

| (b) Submodule 1, 2, 3 undertakes the same PWM time respectively in the positive and negative half cycle |
| M1  | P | 1 | 1 | 1 | 1 | P | P | -1 | -1 | -1 | -1 | P |
| M2  | 0 | P | 1 | 1 | P | 0 | 0 | P | -1 | -1 | P | 0 |
| M3  | 0 | 0 | P | P | P | 0 | 0 | 0 | P | P | 0 | 0 |
| t   | t0~t1 | t1~t2 | t2~t3 | t3~t4 | t4~t5 | t5~t6 | t6~t7 | t7~t8 | t8~t9 | t9~t10 |

| (c) Submodule 1 and 3 have the same modulation time in each cycle |
| M1  | P | 1 | 1 | 1 | 1 | P | 0 | 0 | P | P | 0 | 0 |
| M2  | 0 | P | 1 | 1 | P | 0 | 0 | P | -1 | -1 | P | 0 |
| M3  | 0 | 0 | P | P | P | 0 | 0 | 0 | P | P | -1 | -1 |
| t   | t0~t1 | t1~t2 | t2~t3 | t3~t4 | t4~t5 | t5~t6 | t6~t7 | t7~t8 | t8~t9 | t9~t10 |

The M1, M2, and M3 in the above table represent the cascaded submodule 1, 2, and 3 respectively. P indicates the PWM operation mode. In the arrangement mode 1, the submodule 1 is always in the high frequency modulation mode in one cycle. The advantage of the modulation method is as follows: Switching devices with different withstand voltages can be used in a circuit topology, and greatly reduce the number of switching operations. However there are problems of voltage unbalance and complexity of the control strategy; in arrangement mode 2, each submodule in the four time segment...
of a cycle have the same working time, but the working time is completely different between submodules, voltage balance is not easy to achieve; mode 3 whose positive/negative semi-axisymmetric working mode well balances the working time between modules and can reach the ideal state. Based on this, the control method of this paper adopts the way of combination 3.

**Double Closed Loop Control Strategy of PET**

From the topology of figure 1, the input stage dynamics of PET can be derived as:

\[
\begin{align*}
L \frac{di}{dt} &= u_s - u_{an} = u_s - \sum_{i=1}^{n} u_{dc,i} \\
C \frac{du_{dc}}{dt} &= i_L - i_{L,i}
\end{align*}
\]  

(5)

The conventional control strategy of PET mostly adopts the double closed-loop PI control strategy based on decoupling of dq, but it has the problems of steady state error and anti-interference ability. Quasi-PR control, is also known as quasi-proportional resonance control, considering that PR controller has a narrow frequency band on the basis of proportional resonance and is too sensitive to fluctuations and the response speed and effect are not ideal, so the cut-off frequency is added. The transfer functions of two types of controllers are:

\[
\begin{align*}
G_1(s) &= K_{p1} + K_{r1} \frac{s}{s^2 + w_0^2} \\
G_2(s) &= K_{p2} + K_{r2} \frac{s}{s^2 + 2w_c s + w_0^2}
\end{align*}
\]  

(6)

![Figure 3. Block diagram of double closed-loop.](image)

Based on the above analysis, the double closed-loop control system of the PET is shown in figure 3. The above mentioned PI control of the voltage outer loop and the fundamental quasi-PR control and the third harmonic cancellation of the inner current quasi-PR control will gain the ideal adjustment expectation.

**Simulation Analysis**

In order to verify the optimization strategy proposed in this paper to reduce the switching frequency of the primary rectifier stage of PET, a four module cascaded power electronic transformer simulation model basing on MATLAB/SIMULINK is built. The main circuit structure frame is shown in figure 1, specific simulation parameters are shown in the following table:

In the control process, the reference value of the total DC voltage at the rectifier stage is 1400V; the parameter of the voltage outer loop PI controller $K_p=0.012$, $K_i=4.11$; the parameter of the current inner loop quasi-PR controller $K_p=80$, $K_R=50$; cut-off frequency is elected as $w_c=5\text{rad/sec}$,
Table 2. Parameters of PET.

<table>
<thead>
<tr>
<th>System parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of cascaded modules</td>
<td>4</td>
</tr>
<tr>
<td>Input grid voltage</td>
<td>800V</td>
</tr>
<tr>
<td>Input grid frequency</td>
<td>50Hz</td>
</tr>
<tr>
<td>CHB dc voltage</td>
<td>350V</td>
</tr>
<tr>
<td>CHB carrier frequency</td>
<td>2K Hz</td>
</tr>
<tr>
<td>Input filter inductance</td>
<td>8mH</td>
</tr>
<tr>
<td>CHB dc capacitance</td>
<td>8000uF</td>
</tr>
<tr>
<td>Transformer ratio</td>
<td>1:1</td>
</tr>
<tr>
<td>Secondary resistance</td>
<td>20Ω</td>
</tr>
<tr>
<td>DAB switch frequency</td>
<td>1250Hz</td>
</tr>
</tbody>
</table>

Figure 4. DC voltage of submodule.  
Figure 5. Total DC voltage of cascaded rectifier stage.

Figure 4 shows the simulation of the DC voltage waveforms of the four submodules of the PET primary rectifier stage, and figure 5 shows the total voltage waveform of the DC side. It is very intuitive to see that the total voltage on the DC side can be stabilized at a set reference value of about 1400V, which verifies the rationality of the parameter design of the voltage outer loop PI controller.

Figure 6. Modulated voltage of hybrid pulse width modulation.  
Figure 7. Multi-level synthesis voltage $u_{an}$.

Figure 6 above shows the reference voltage waveform output by the dual loop controller. The reference voltage is approximately sinusoidal, and the peak value is kept at around 1100V, figure 7 shows the synthetic voltage waveform with hybrid pulse width modulation.

The following figure (a) shows the grid-side voltage and current waveforms. Figure (b) is the amplification effect diagram of the current in the grid-side, from which it can be seen directly that the grid current is good enough under the corresponding double closed-loop control strategy.
It can be seen from the simulation results that the grid-side current distortion ratio is only 1.42%, and the sinusoidal characteristic is good. The harmonics are mainly distributed in 40, 80, 120 times nearby. It can be seen that the distortion ratio of the composite voltage is 15.36%, and the harmonics are mainly concentrated near 40, 80, 120 times, that is, the number of harmonics. It is pF+q (F is the carrier ratio, and the carrier ratio in this paper is 40), where p and q are greater than 0, according to the reference [3], the distortion of output multilevel voltage under the author's hybrid pulse width control strategy is 16.88%, so the output voltage distortion rate under the control strategy of this paper is smaller and has obvious advantages.

By running this model, the voltage peak of the power grid can be 1131V, the network side current is 45.11A, and the active power P is 25.52KVA, the power Q is 168.4 var, and the distortion rate THD of grid-side current is 0.2499. According to this, the following formula can be used:

\[ v = \frac{1}{\sqrt{1 + THD^2}} = \frac{1}{\sqrt{1 + 0.2499^2}} = 0.97017 \]  

(7)

\[ \cos \Phi_i = \frac{P}{\sqrt{P^2 + Q^2}} = \frac{25520}{\sqrt{25520^2 + 168.4^2}} = 0.99998 \]  

(8)

\[ \lambda = V^* \cos \Phi_i \approx 0.9702 \]  

(9)

The power factor of the network supply is 0.9702, which is close to the unity power factor operation, and the power supply efficiency is very high, achieving ideal control expectation.

**Summary**

In this paper, a possible sorting list of the working status is targeted for research according to study of hybrid pulse width modulation strategy, and the quasi-PR control substituting the conventional PI control in the current inner loop is proposed, and the optimal solution is finally determined. The simulation results show that the determined scheme can greatly reduce the switching times of the rectifier stage, maintain the approximate unity power operation. The synthesized multilevel voltage
harmonics are of good characteristics and have great advantages, thereby high performance is obvious.

References


