A Low Power Single Ended Inductorless Wideband CMOS LNA with $G_m$ Enhancement and Noise Cancellation

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Abstract. This work proposes a low power single ended wideband CMOS low noise amplifier for low power short-range wireless communication based on IoT. The main novelty lies in significant improvement in bandwidth by using the inverter cell and in noise by noise cancellation topologies. By using active shunt-feedback architecture, the current of the feedback stage is reused on the forward path to improve the current efficiency of the LNA. The complementary characteristic leads to partial second-order distortion cancellation simultaneously. With TSMC 180 nm CMOS process, the proposed LNA presents maximum voltage gain of 15 dB, a minimum noise figure of 1.79 dB and an input 1 dB compression point of -24.65 dBm. It consumes 3 mW from 1.8 V dc supply and occupies a core area of 0.004 mm².

Introduction

With the progress of modern science and technology, various wireless communication technologies of Internet of Things (IoT) have been rapidly developed. At the same time, there are more stringent requirements for the performance of wireless communication technologies. As the important part of the wireless communication system, low power and small size wireless transceivers have attracted great study efforts. The low noise amplifier, as the first active block in the front-end of RF receiver, has to provide an enough signal-to-noise ratio for the following block, wideband input impedance matching, high gain, low noise, and modest linearity simultaneously.

The design of low power wideband low-noise amplifiers has been an active research topic (e.g. [1-5]). In [1], a common-gate LNA with dual cross-coupled capacitive feedback is present by H. G. Han. The LNA realizes low power consumption and a high gain. However, it does require an off-chip balun, which increase cost and impedes full system integration. The LNA presented by H. Rashtian in [2] adopts body biasing in each stage to adjust gain variation independently, but this is achieved at the cost of high noise degradation. In the LNA present by M. De Souza in [3], the use of current-reuse technique leads to achieve both high gain and low power consumption, but with a high noise figure compared to that achieved in this work. The LNA depicted by M. Parvizi in [4] combines complementary current-reuse and forward body biasing (FBB) to realize a very low voltage and ULP LNA, however, this comes at the cost of a large number of inductors and a large chip area. Z. Pan presents an inductorless low power differential low-noise amplifier in [5]. The LNA utilizes a cross-coupled push-pull structure to realize $G_m$ boosting and partial noise cancelling, but it increases the power consumption of the LNA 2mW.

In this work, we introduce a low power single ended inductorless wideband CMOS LNA with complementary current-reuse and noise cancellation. Based on the combination of common-source (CS) and common-gate (CG) with active shunt feedback topologies, the LNA realizes $G_m$ boosting and partial noise cancelling under low power consumption.

This paper is organized as follows. In Section 2, circuit description of the proposed LNA will be introduced and analyzed. The measurement results are provided in Section 3, and a conclusion is presented in Section 4. Finally, an acknowledgement expresses my gratitude to the foundation that supports this work in Section 5.
**Proposed LNA**

Shown in Fig. 1 is the proposed LNA schematic, consisting of a CS input stage with resistor feedback and a CG stage with active shunt feedback. The CS stage is a complementary current-reuse structure, which improves the effective input transconductance, and further increases gain without increasing the dc power consumption of the circuit. Moreover, the feedback resistor $R_F$ provides the self-biased voltage for the NMOS and PMOS, eliminating the need for additional dc power.

In the second-stage, adjusting the transistor threshold voltage through FBB reduces the $V_{gs}$. In order to further reduce the $V_{gs}$ required, MOSFETs operate in weak inversion [4]. The NMOS and PMOS transistors are turned over so that the current of the transistors M5 and M6 in the shunt feedback loop is reused by the forward path transistors M1 and M2 to increase current efficiency and reduce power consumption. M3 and M4 are active load impedances, which facilitates maintaining a constant impedance at the low $V_{ds}$ and increasing the voltage margin of M1 and M2.

![Figure 1. Schematic of the proposed LNA.](image1)

**Input Impedance**

To find the input impedance, the small-signal schematic of the proposed LNA shown in Fig. 2 is analyzed. Assuming at the operating frequency, the capacitive effects of transistors are not significant, and the following expressions are obtained

$$Z_{in1} = \frac{1}{(G_M Z_{in2})/(R_F + Z_{in2})}$$

$$Z_{in2} = \frac{1}{((1/(g_{o3}+g_{o4}))-2g_{o1})/(G1+G2)(1+A)}$$

Where $G_M = G_{MN} + G_{MP}$, $G_{MN} = g_{mn} + g_{on}$, $G_{MP} = g_{mp} + g_{op}$, $G_1 = g_{m1} + g_{o1}$, $G_2 = g_{m2} + g_{o2}$, $R_F$ is the feedback resistor, $g_{oi}$ is the output conductance of transistor $M_i$, and $A = (g_{m5} + g_{m6})/(g_{o3} + g_{o4})$.

Compared with the conventional CS or CG circuit, the effective $G_M$ is much larger with the same power consumption. It is clearly shows that the shunt feedback network boosts the effective $g_m$ by a factor of $(1 + A)$. All of these transconductance enhancement techniques allow the circuit to improve the dc power tradeoff for gain and impedance matching.

**Voltage Gain**

Assuming that V2 and V3 are ideally ac coupled together through C1, the voltage gain ($A_V$) for Fig. 2 is given by Eq. 3 and Eq. 4 respectively.

$$A_V1 = \frac{(G_M \cdot G_{MP})/(1+RF) \cdot (G_{MN}+G_{MP})}{(G_{MN}+G_{MP})}$$

$$A_V2 = \frac{(r_{o3} \cdot r_{o4})/((1+A) \cdot G + (r_{o3}+r_{o4}))}{(1+A)}$$

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Where \( G = G_1 + G_2 = g_{m1} + g_{m2} + g_{o1} + g_{o2} \), \( A = (g_{m5} + g_{m6})/(1/(g_{o3} + g_{o4})) \), \( r_o \) is the output resistance of transistor \( M_i \). Eq. 2 and 4 highlight the fundamental tradeoff between good impedance matching and high gain. The factor of \((1+A)\) introduced by the shunt feedback network makes it easier to improve impedance matching, but at the cost of lower voltage gain.

**Noise**

Fig. 3 shows the proposed LNA with noise contributed from only M1 for simplicity. \( r_{o3} \) and \( r_{o4} \) are the equivalent load resistance of the transistors M3 and M4, respectively. The channel thermal noise current of M1, \( I_{n1} \), flows along the load resistance \( r_{o3} \) and source resistor \( R_s \) thus creates a noise voltage at V2 and a correlated noise voltage with a smaller amplitude and opposite phase at V1. The noise voltage at V1 is amplified by M2 and appears at node V3. If V2 and V3 are ac coupled together, the noise voltages on V2 and V3 which have opposite phases are added together and the noise from M1 will be cancelled. The noise-cancellation mechanism also applies to the noise generated by M2.

![Figure 3. Noise mechanisms in the LNA.](image)

**Linearity Analysis**

For low-noise amplifiers, the main reason for the signal distortion is that the process of converting the input voltage into an output current through transconductance is non-linear. The nonlinearity of the CG stage of proposed LNA is analyzed using a Taylor series. The output current of the input stage without the shunt transistors M5 and M6 can be characterized by the first three terms of a Taylor series as proposed in Eq. 5.

\[
\text{i}_{\text{out}} = -a_1 v_{gs} + b_1 v_{ds} + a_2 v_{gs}^2 + b_2 v_{ds}^2 - a_3 v_{gs}^3 + b_3 v_{ds}^3 \tag{5}
\]

Where \( a_1 = g_{m1} + g_{m2}, b_1 = g_{ds1} + g_{ds2}, a_2 = (g_{ds2} - g_{m1})/2, b_2 = (g_{ds1} + g_{ds2})/2, a_3 = (g_{m2} + g_{m3})/6, \) and \( b_3 = (g_{ds1} + g_{ds2})/6 \). \( g_{m1} \) and \( g_{m2} \) are the first- and second-order derivatives of \( g_{m} \) with respect to \( V_{gs} \). \( g_{ds1} \) and \( g_{ds2} \) are the first- and second-order derivatives of \( g_{ds} \) with respect to \( V_{ds} \). From the coefficient \( a_2 \) can be seen that the complementary characteristics of NMOS and PMOS transistors can contribute to cancellation of second-order distortion.

**Experimental Result**

The proposed LNA is implemented in a 1P8M 180 nm TSMC CMOS process. A layout of it is shown in Fig. 4. The entire LNA occupies an area of 0.14 mm² mainly determined by the pad, and the core area is only 0.004 mm². The LNA consumes 3 mW from a power supply of 1.8 V.

The measured voltage gain and NF, along with post layout simulation (PLS) results, are shown in Fig. 5. The LNA achieves an S21 of 14.38 dB at 2.4 GHz and the maximum S21 of 15 dB with a -3 dB
BW of 0.09-2.64 GHz. As can be seen, the NF is below 5 dB between 0.2-3.3 GHz and the NF is 1.799 dB at 2.4GHz. The linearity of a LNA is usually characterized by the 1 dB gain compression or the third-order intercept point (IP3). The input–output characteristics of the LNA are shown in Fig. 6. The 1 dB compression point is at -24.65 dBm.

The performance of the LNA is summarized in Table 1 and is compared with state-of-the-art works. A figure of merit (FoM) is used to compare the overall performance of the LNAs and given by Eq. 6[11]. The LNA presented here offers comparable performance in terms of gain, NF, and linearity, which leads to achieving one of the highest FOM.

\[
\text{FOM} = \frac{(G(dB) \cdot BW(GHz))}{(\text{NF(dB)} - 1 \cdot Pdc(mW))}
\]  

Table 1. Performance Summary and Comparison.

<table>
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<tr>
<th>Parameter</th>
<th>This Work</th>
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<td>2-11.5</td>
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<td>0.4-1</td>
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<td>21.3</td>
<td>0.2</td>
<td>8.5</td>
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<td>Gain(dB)</td>
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<td>17.5</td>
<td>15.5-18</td>
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<td>NF(dB)</td>
<td>1.79</td>
<td>2.8-3.4</td>
<td>3.5</td>
<td>3.1</td>
<td>2.9-3.5</td>
<td>4.2</td>
<td>4.3</td>
</tr>
<tr>
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<td>0.33</td>
<td>-</td>
<td>0.27</td>
<td>0.86</td>
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<td>2.6</td>
<td>4.99</td>
<td>0.7</td>
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</table>

Conclusion

The design and implementation of an inductorless, low power wideband LNA is presented. The proposed topology suits to low power short-range wireless communication based on IoT. In this work, taking advantage of a current-reuse technique achieves both high gain and low power consumption. The use of active shunt-feedback complementary structure contributes to partial noise and harmonic distortion cancellation. An FBB scheme was used to reduce the overall dc current in the amplifier. The LNA was implemented in a 1P8M 180 nm TSMC CMOS technology. The measured LNA has a 15dB gain, 1.8 dB minimum noise figure, an input 1dB compression point of -24.44 dBm and 0.09-2.64 GHz bandwidth, while consuming only 3 mW of power from a 1.8 V supply. The layout area occupied is 0.004 mm².
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References


