Loss Optimization Method Based on the Main Circuit of T-type SVPWM

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Keywords: T-type Three-level, IGBT, 7-segment SVPWM, 5-segment SVPWM, Switching Loss.

Abstract. To reduce the switching loss of power devices and improve the efficiency, an effective method is to reduce the switching loss by optimizing the modulation strategy of the control algorithm. Traditionally, the amount of on-off times is used to qualitatively estimate the amount of switching losses, but the estimation error is large. In this paper, based on a T-type three-level topology, the 7-segment and 5-segment SVPWM strategies were analyzed theoretically, the calculation methods were set, and an experiment is carried out on a high-power frequency conversion system. It is proved that the reduction amount of switching losses of power devices is not only determined by the reduction amount of switching times under different modulation strategies.

Introduction

With the development of modern power electronics technology, using IGBT, the SVPWM Variable-Frequency Adjustable-Speed system has been widely used [1]. However, due to the restriction of power devices, and the complex structures, the system losses cannot be ignored [2]. The total loss can be divided into two parts: conduction loss and switching loss. Switching loss is the main factor of power losses, which can restrict the working efficiency [3]. If the power devices have been identified, the switching loss of IGBT can be reduced by changing 7-segment into 5-segment SVPWM [4]. The on-off times can be reduced from 6 to 4 times in a control period, and the reduction rate was 1/3. Traditionally, it is thought that the amount of switching losses can be reduced by 1/3, too. However, the switching losses are different in each on-off time of a period, the amount of on-off times cannot reflect the total switching losses directly.

In reference [2], the advanced discontinuous 5-segment space vector pulse has lower switching losses compared with the traditional 7-segment. In reference [3] and [4], based on a T-type three-level topology and a three-level neutral-point clamped (NPC) topology, it is shown that the switching losses of IGBT are lower under 5-segment SVPWM by simulation [5]. However, after optimizing the modulation strategy, the actual reduction rates still need to be further specify.

In this paper, to prove that the amount of IGBT switching losses cannot be estimated only by the amount of on-off times, based on a T-type three-level topology, the loss calculation methods were provided, and an experiment was carried out in a high-power T-type three-level inverter.

Loss Analysis and Calculation Method

Loss Analysis

The three levels at the output side, P, O, N, can be obtained through different on-off states of the 4 IGBT devices of each phase [6]. Compared with the neutral point clamped one, T-type three-level inverter uses fewer devices, a common-collector circuit and needs only 5 drive power supplies, has a great practical value [7]. The topology is shown in Figure 1.
The circuit uses three-level SVPWM as the modulation mode. Taking the 1st sector as an example, according to the principle of combining the three-adjacent vector, assume that the output line voltage vector \( v_{01} \) is in area B, and the neutral of the capacitor, 0, is the reference potential, the first acting vector is a positive small vector \([8]\), under the strategies of 7 and 5-segment SVPWM, the space vector modulation sequences of \( U \), \( V \), and \( W \) phases are shown in Figure 2. In area B, after changing the control algorithm from 7 to 5-segment, the switching loss changes of \( U \), \( V \) and \( W \) are shown in Table 1.1, where \( E_{on} \) and \( E_{off} \) are the amount of turn-on losses and turn-off losses of main switch, and \( E_{aux-ref} \) is the reverse recovery loss of auxiliary free-wheeling switch.

![Figure 1. T-type three-level converter topology.](image1)

![Figure 2. Sequence waveforms of area B.](image2)

<table>
<thead>
<tr>
<th>Bridges</th>
<th>Increase</th>
<th>Decrease</th>
</tr>
</thead>
<tbody>
<tr>
<td>U</td>
<td>t1/2 turn-on time of Upper switch</td>
<td>( E_{on} ) and ( E_{off} ) of main, ( E_{aux-ref} ) and t1/2 turn-on time of Aux switch</td>
</tr>
<tr>
<td>V</td>
<td>t1/2 turn-on time Aux switch</td>
<td>t1/2 turn-on time of lower switch</td>
</tr>
<tr>
<td>W</td>
<td>t1/2 turn-on time Aux switch</td>
<td>t1/2 turn-on time of lower switch</td>
</tr>
</tbody>
</table>

**New losses calculation method**

**Switching Loss.** In the common collector circuit, it is related to the collector-emitter(CE) voltage \( V_{ce} \), the collector current \( I_c \), and junction temperature \( T_j \). Assume the switching frequency of the device is \( F_{sw} \), the expression of switching losses of IGBT is shown in Formula 2.

\[
P_{sw} (t) = f_{sw} \sum_{i=1}^{n} (E_{on}(V_{ce}, I_c, T_j) + E_{off}(V_{ce}, I_c, T_j))
\]

(1)

Reading out the rated amount of turn-on loss and turn-off loss under the corresponding operating temperate of IGBT in Datasheet, and considering the differences between actual current and reference current [9], the expression of switching losses of IGBT is shown as follows.

\[
P_{sw} (t) = \frac{1}{T} \sum_{i=1}^{n} (E_{on} + E_{off} \times \frac{I_k}{I_{ref}} \times \frac{K_{sw-I1}}{V_{ref}})
\]

(2)

where \( T \) is the control period; \( n \) is the on-off times; \( E_{on} \) and \( E_{off} \) are the rated turn-on and turn-off losses under the condition that the driving resistance, driving voltage, reference CE voltage \( V_{ref} \), and reference collector current \( I_{ref} \) are given; \( I_k, V_k \) are the peak collector current and CE voltage under the switching period. The influence coefficient of the collector current amplitude and the CE voltage amplitude, \( K_{sw-I1}, K_{sw-I2} \) are determined to be 1 and 1.3.

The characteristic of the anti-parallel diode can be read out in the Datasheet. The expression of the switching losses of anti-parallel diode is shown as follows [10].
\[
P_{sw} = \frac{1}{T} \sum_{i=1}^{n} (Q_{rr-ref} \cdot \left( \frac{I_k}{I_{ref}} \right)^{K_{sw-D1}} \cdot \left( \frac{V_k}{V_{ref}} \right)^{K_{sw-D2}} \cdot V_d) \tag{3}
\]

where \(Q_{rr-ref}\) is the reverse recovery charge under the condition that the reverse recovery voltage, forward conducted current, and junction temperature is given. The influence coefficient of forward conduction current amplitude and reverse recovery voltage, \(K_{sw-D1}, K_{sw-D2}\), are 0.6 and 0.6.

**Conduction loss.** By taking the product of the instantaneous turn-on voltage \(v_{ce}(t)\) and the instantaneous collector current \(i_c(t)\), the instantaneous value of the conduction loss can be obtained. By integrating the instantaneous value in a period, the conduction losses can be obtained \([11]\).

\[
P_{cond}(t) = \frac{1}{T} \int_{0}^{T} i_c(t) \cdot v_{ce}(t) dt \tag{4}
\]

Assume that \(V_{ceo}\) is the turn-on voltage of conduction fitting curve, \(r_{ce}\) is the conduction bulk resistor, and \(I_{cm}\) is the peak rated current \([12]\). Under the working temperature of IGBT, according to the conduction curve at the corresponding temperature, and doing an approximate straight-line processing to \(V_{ceo}\) and \(r_{ce}\), the expression of IGBT’s conduction losses can be concluded as follows.

\[
P_{cond}(t) = \frac{1}{2\pi} \int_{0}^{2\pi} (V_{ceo} + r_{ce} \cdot I_{cm} \cdot \cos(\theta)) \cdot I_{cm} \cdot \cos(\theta) d\theta \tag{5}
\]

**Simulation Analysis**

In this paper, a simulation model was built in MATLAB / SIMULINK environment. The DC power voltage \(V_{DC}\) of the model is 200V, the DC bus capacitor of neutral point \(C\) is 220 \(\mu\)F, and on-off frequency \(f_s\) is 20 kHz.

The space vector modulation sequence diagram of 7 and 5 segment are shown in Figure 3. It can be obtained under 5-segment, there exist a straight, no chopped voltage waveform. In an area of the sector, the switching elements of that phase can be led not to switching, which can reduce the switching frequency, and eliminate the switching losses of that phase.

![Figure 3. SVPWM sequence waveforms.](image1)

![Figure 4. Test sample machine.](image2)

**Experimental Results and Analysis**

A high-power T-type three-level inverter is used as an experimental object to do a practical engineering calculation of switching losses. The picture of test sample machine is shown in Figure 4.
The calculation model is a 15kW T-type inverter. The IGBT power tube, IKW40N120H3, IKW75N60T, made by Infineon, are chosen as the main power switch and auxiliary free-wheeling switch. The list of main parameters of the system is shown in Table 2. Before calculating, the 50% maximum peak to peak ripple current should be considered.

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Value (Unit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Power $P$</td>
<td>15(kW)</td>
</tr>
<tr>
<td>DC Bus Voltage $V_{DC}$</td>
<td>720(V)</td>
</tr>
<tr>
<td>Rated Output Voltage RMS $V_o$</td>
<td>400(V)</td>
</tr>
<tr>
<td>Rated Output Voltage Frequency $f$</td>
<td>50(Hz)</td>
</tr>
<tr>
<td>Switching Frequency $f_s$</td>
<td>20(kHz)</td>
</tr>
</tbody>
</table>

Table 2. List of experimental platform parameters.

Figure 5. Ripple current waveform

7-segment SVPWM

In main switch, the amount of each IGBT switching losses, each anti-parallel diode switching losses, the six switching devices totally are $P_{sw-I1-7}$, $P_{sw-D1-7}$, $P_{sw-1-7}$. In auxiliary switches part, the amount of switching losses of each IGBT, each anti-parallel diode, and the six switching devices totally are: $P_{sw-I2-7}$, $P_{sw-D2-7}$ and $P_{sw-2-7}$. The amount of total switching losses is $P_{sw-7}$. By Math-CAD, the results of each variable on the experimental platform are shown in Table 3.

5-segment SVPWM

When the voltage utilization is high, the duration of the vector when it is in area C is very short. So, the on-off time can be ignored, which will not affect the actual results. In area A, the reduction amount of each main power IGBT, each auxiliary IGBT, each auxiliary anti-parallel diode, total switching losses of the six switching devices are $\Delta P_{sw-IA1-5}$, $\Delta P_{sw-IA2-5}$, $\Delta P_{sw-D2-5}$, $\Delta P_{sw-A-5}$. Similarly, in area D, the reduction amount of switching losses of main power IGBT, each auxiliary IGBT, each auxiliary anti-parallel diode, and the six switching devices totally are $\Delta P_{sw-ID1-5}$, $\Delta P_{sw-ID2-5}$, $\Delta P_{sw-DD2-5}$ and $\Delta P_{sw-D-5}$. The total reduction amount of switching losses is $\Delta P_{sw-5}$. The results of each variable on the experimental platform are shown in Table 4. Here, the reduction quantity of conduction losses of IGBT, $\Delta P_{cond-5}$, is also calculated, which is 13.662W.

Table 3. Switching losses of 7-segment SVPWM. | Table 4. Losses reduction quantities of 5-segment SVPWM.

<table>
<thead>
<tr>
<th>Main</th>
<th>$P_{sw-I1-7}$</th>
<th>18.145(W)</th>
<th>$\Delta P_{sw-IA1-5}$</th>
<th>1.688(W)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$P_{sw-D1-7}$</td>
<td>3.302(W)</td>
<td>$\Delta P_{sw-D2-5}$</td>
<td>0.943(W)</td>
</tr>
<tr>
<td></td>
<td>$P_{sw-1-7}$</td>
<td>128.736(W)</td>
<td>$\Delta P_{sw-A}$</td>
<td>18.648(W)</td>
</tr>
<tr>
<td></td>
<td>$P_{sw-I2-7}$</td>
<td>4.254(W)</td>
<td>$\Delta P_{sw-ID1-5}$</td>
<td>1.064(W)</td>
</tr>
<tr>
<td></td>
<td>$P_{sw-D2-7}$</td>
<td>7.847(W)</td>
<td>$\Delta P_{sw-ID2-5}$</td>
<td>0.733(W)</td>
</tr>
<tr>
<td></td>
<td>$P_{sw-2-7}$</td>
<td>72.606(W)</td>
<td>$\Delta P_{sw-DD2-5}$</td>
<td>0.023(W)</td>
</tr>
<tr>
<td></td>
<td>$P_{sw-7}$</td>
<td>201.342(W)</td>
<td>$\Delta P_{sw-D-5}$</td>
<td>10.920(W)</td>
</tr>
<tr>
<td>Total</td>
<td>$P_{sw-7}$</td>
<td>201.342(W)</td>
<td>$\Delta P_{sw-5}$</td>
<td>29.568(W)</td>
</tr>
</tbody>
</table>
The reduction rate of switching losses, $\eta_{sw}$, of the inverter is shown in Formula 6. Ignored the effect of harmonics on the losses of the magnetic component, measured the output power at output side, $P_0 = 0.95P_N$, the enhanced efficiency, $\Delta\eta$, is shown in Formula 7.

$$\eta_{inv-sw} = \frac{\Delta P_{sw-5}}{P_{sw-7}} = \frac{29.568}{201.342} = 14.685\%$$  \hspace{1cm} (6)

$$\Delta\eta = \frac{\Delta P_{sw-5} + \Delta P_{cond-5}}{P_o} = 0.302\%$$  \hspace{1cm} (7)

The reduction rate of switching losses is not 1/3, but 14.685%. And the efficiency of the inverter is enhanced by 0.302%. In the practical engineering application, the results corrected the original idea. Meanwhile, when reducing the switching frequency, the 5-segment SVPWM can also cause more harmonics, which increases the difficulty of the inverter development.

**Summary**

Based on a T-type three-level topology, it can be confirmed that the reduction rate of switching losses cannot be qualitatively estimated by the reduction rate of on-off times. When changing the modulation strategy, the reduction rate of switching losses is lower than estimated one’s. The reduction values vary with different devices. In actual power design, it is necessary to calculate the losses according to the specific experimental models, then, there will be a more accurate losses data. The losses calculation method of power devices was proved by practical test. It can guide the efficiency design of power electronic products and optimize circuits better in practical applications.

**Acknowledgement**

This paper is partially aided by Natural Science Foundation of China (61503224, 61305129), Shandong Province Natural Science Foundation (ZR2016EEP10), Shandong Graduate Education Innovation Program (SDYY16002, SDYY17035), 2016 Graduate Education Innovation Program project of Shandong University of Science and Technology.

**References**


