Methodological Research on Testability Design for Microcontroller
Shui-rong JU, Shuo BAI, Kai-peng GUO, Jia LI and Ling-zhi KONG
Jiangsu College of Information Technology. Wuxi Jiangsu, 214153, China

Keywords: Embedded-system, Design for testability, Instruction.

Abstract. Two methods about design for testability are given. Design for testability about calculator circuit SX1702 which based on 4-bit embedded-system are introduced include module division and ROM content testing, this technique provides both controllability and observability.

Introduction
SX1702 is a powerful 4 bit embedded micro controller (MCU) which has been widely used. However, all the functions completed by this circuit are all decided by instructions of ROM inside the chip. Abundant instruction systems but with less IO pins for SX1702 resulting in poor controllability and observability. So Design for testability is very important for this type MCU, and several methods for testability will be introduced in this paper.

Accurate Module Partition and Internal Data Bus
Make the whole circuit divide into modules and make these modules work in different states by external control signal is one of the effective methods to improve testability. The SX1702 calculator circuit make a detailed consideration in this respect. It has four Test input TS1~TS4, through these input we can make different modules in different states. The overall functional block diagram of SX1702 is shown in Figure 1.

![Block diagram of embedded micro-controller circuit.](image)

The micro-controller circuit diagram in figure 1 shows the kernel part and the peripheral module, among the peripheral module includes keyboard interface, LCD driver, voltage doubling circuit, oscillator, and clock module. We can set several input pins for different states. To make the whole
circuit into Normal working mode, System reset mode, System wait mode and System test mode, etc. What’s more, the internal modules works differently under these operating modes, which makes the whole circuit has good Controllability and observability, also provides favorable conditions for chip testing.

In order to perform high efficient testing on calculator chips based on micro-controller, we must build effective internal date bus architecture in the design bus. In the circuit design phase, we should not only make sure the circuit has normal functions, but also need to contain some Structure modules be used for testing. These modules do not work when the circuit works normally, they works only when the circuit under the test state, to complete the test. Figure 1 shows Chip internal data bus architecture for compatible with testability design Which includes:

1. represents express values on the internal data bus enter ALU;
2. represents values on the internal data bus enter program counter and produce the address of the next instruction;
3. represents values on the internal data bus control Liquid crystal display decoder;
4. represents putting operation results on the internal data bus;
5. represents instruction decode data enters into internal data bus through the internal data bus.

Scanning Test Method

Random Access Scan

The technology of random access scan has the advantages of complete controllability and observability for memory element in circuit. This kind of method don’t needs to shift register, but need address programmable module to make sure all the internal memory element can be uniquely selected for being control and been observed the mechanism of the programmable address is just similar to RAM. Figure 2 show us a sketch Map of system configuration using a random access scan method, including Y address, X address, a decoder, Address programmable storage element, System clock, Protection Counter Functions and so on in Figure 2.

Method for Reducing Interference Scanning Path

Scanning (as well as scanning related) methods have some advantages for global structured test generation and testing techniques. However, this method will increase the cost of the product, and for the long test of time required to scan design will also increase the test time, this will also affect the amount of the product, which leads to reduce the interference method of scanning path.

By using the method of reducing the interference scanning path, the key control and observation points in the circuit can be uniquely identified, and the observation point can be controlled and
observed by using a testability unit (a "test unit"), then these test units connect serially, similar to scan chain, allowing the transfer of information between the nodes of the key cells in the test state. Compared to full scan technology, using this method requires only a little increase in I/O and chip cost. Figure 3 shows the test unit added to the design for testability.

Figure 3. The test unit added to the design for testability.

In figure 3, DI is a normal data input, and DO is a normal data output. In normal working condition, the multiplexer in Figure 3 on the right will be set, the DI data will get directly to the DO without affecting the circuit work through the test enable terminal ENS. In the test, if we select appropriate test clock CLK, Scan input SI and scan enable ENS, then the data can be reached on the selected node, which means the data will enter into the “test unit” by scanning the input SI, through the Test enable side ENT and finally get to DO, replaces the date under normal working conditions.

Built in Self Test (BIST) Technology

Built in self test technology is a kind of technology put test excitation test result detection in the same chip, using this technology, as long as there is one test result of the output line to the chip output pin can determine whether there is a fault in the chip, in addition, we can also add fault correction circuit in the chip automatic correct some faults in the circuit. BIST has two stages, the first is adding the test sequence produced in test signal generator to the circuit under test, then the test result analyzer will check the output of circuit under test to see whether there is a fault.

In this paper for SX1702, BIST is used for program memory in Figure 4.

In Figure 4 CK is the clock; A[M-1:0] is address input; Q[N-1:0] is data output; BIST is self test mode control signal; BFD is self test sign detection signal; BC is self test completion indication signal; BF is self test marks. The algorithm used by program memory with self test is a combination of exhaustive test of pattern generation and feature analysis technique, using this algorithm can make the fault coverage above 99%.

Figure 4. Diagram of self test program memory in the SX1702.

When it’s in the time slot D, if the output signal is “1”, means there is a ROM fault; when it’s in the time slot E, BFC jumps into “1”, makes BF becomes “1”, then the output stack-at-0 has a fault. You may think carefully about the two parts of the algorithm above, namely, the produce of test stimulus and the compare of test results, we will make detailed introduction behind.
Conclusion

The calculator circuit based on embedded MCU must be considered the testability design in the early stage of chip design, the ROM content can be read and make the circuit’s different modular work in different states through module division and input combination to raise the controllability and observability of chips and shorten the test time.

Acknowledgements

This research is supported by the Top-notch Academic Programs Project of Jiangsu Higher Education Institutions(PPZY2015B190),it is also supported by the project of Science and technology innovation team for “Blue Project” of Education Department Jiangsu Provinces.

References


