Memristor Based Quantization Circuit Design for ADCs

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Keywords: Memristor, SPICE model, Quantization circuit.

Abstract. As the fourth fundamental circuit element, memristor will introduce great change to the conventional electronic circuits. Quantization circuit of ADC (Analog to Digital Converter) is one of the promising circuits applications that can be improved by memristors. In this manuscript, a parallel memristors quantization circuit design is proposed. The circuit with such implementation scheme is able to achieve high rate and high precision quantization conversion. Compared with other memristor based quantization circuit, it shows good performance in power dissipation and circuit size.

Introduction

Since the ADC (Analog to Digital Converter) is the main block in mixed signal applications, the design requirement for a low power, high speed and wide bandwidth ADC has increased tremendously, which becomes a bottleneck in data processing applications. And the performance of the quantization circuit mostly determines the performance of the ADC. Because the conversion rate, accuracy, and power consumption of the ADC are mainly determined by the quantization circuit part. At present, there is variety of quantization circuits with different CMOS circuit based architecture. The most widely utilized architectures include flash (parallel) ADCs, folding/interpolation ADCs and pipeline ADCs [1]. The fully parallel structure is characterized by high speed, but the resolution is difficult to increase and the power consumption is large. The folding/interpolation type has high resolution, low power consumption, but low speed and difficulty in further improvement. And the speed and resolution of the pipeline structure are relatively balanced, and have almost reached the theoretical upper limits. So it is imperative to study new quantitative circuit architectures based on some emerging devices.

Recently, memristors considered as a new fundamental two terminal circuit devices [2, 3], exhibit the expected advantages in high-density integration, low power consumption, and high-speed read and write [4]. Besides the crossbar architecture of memristor integration can significantly increase memory density while reducing power consumption. It should be highlighted that memristor has been highly considered to be one of the promising candidate for implementation of next generation non-volatile memory, which thus could advance Moore’s Law beyond the present silicon roadmap horizons. Moreover, memristive devices naturally combine the logic, storage and computing function together, which have a wide range of applications, covering almost all existing electronic circuits, and is constantly expanding its application fields [5-7].

Quantization Circuit Design with Memristors

Existing Memristor-based ADC Design

Compared with traditional ADCs, memristor-based ADC designs are characterized by small size, fast conversion speed, and low power consumption. Y.V. Pershin proposed a memristor-based ADC design method which uses the existing sample-and-hold circuit by default, and the quantized coding part is designed [7]. A two-terminal threshold switch memristor is used in the design. This memristor is non-volatile and can record information. When the voltage across the memristor exceeds the
threshold, the memristor is activated and the state transitions. The voltage controlled memristor can be described by the following formula:

\[ I_M = [M(x, V_M, t)]^{-1} V_M \] (1)

\[
\frac{dx}{dt} = f(x, V_M, t)
\] (2)

Where \( I_M \) is the current through the memristor and \( V_M \) is the voltage across the terminals. \( M \) is the memristance value, \( x \) is the internal state variable, and \( f \) is the dynamic function of the device. Assuming that the threshold voltage of the memristor is \( V_{th} \), when \( |V_M| > |V_{th}| \) the \( M \) value will be changed. \( R_{ON} \) and \( R_{OFF} \) are low resistance state and high resistance state, respectively, and the corresponding logic values are 1 and 0.

The published memristor-based ADC circuit and coding scheme are shown in Fig. 1. All the state of memristors in the same column are initially set to "on" (low resistance configuration). A synchronized pulse signal is applied to the two terminals of the memristor. The pulse width is \( T \), and \( T \) is the shortest time that can guarantee changing the state of the memristor when the voltage exceeds the threshold. The amplitude of left pulse is \( V_{in} \) which is the pulse for the input signal sampling. The amplitude of pulse on the right side is \( i\Delta V \), \( i=0, 1, ..., N-1 \). In order to avoid an error when the input voltage is close to the threshold, let \( \Delta V=4/3V_{th} \). The pulse signals on both sides are inverted and synchronously loaded on this series of memristors. Since the voltage difference across the memristor is greater than \( V_{th} \), the memristor will transition from the "on" state to the "off" state. It can be seen that when the first positive pulse acts on the memristor, all memristors with \( j<(V_{in}+V_{th})/\Delta V \) are set to the "off" state (the high resistance state). Since the diode at the right end, which only allows the forward current to pass, the latter negative pulse sets the memristor \( i<(V_{in}-V_{th})/\Delta V \) to the "off" state, i.e. avoiding the memristor that has been converted to the "off" state changing back to "on" state.

When the pulse signal is applied, only one or two adjacent memristors are in an "on" state. Figure 1 b and c show the main steps of the two conversion results.

![Figure 1](image)

Figure 1. a. Existing memristor-based ADC design. b. The main steps of only one memristor in the "on" state after conversion. c. The main steps of having only one memristor in the "on" state after conversion.

Such novel design still have some shortcomings. First, each signal pulse is required to be reversed, which increases the complexity of the VLSI design, and it is very difficult to synchronize the two pulses at the nanosecond level. Second, each ADC requires a series of pulses at the other end of the memristor sequence, which increases the power consumption of the system and weakens the power consumption of the memristor as a passive device. In addition, if a high-resolution ADC is implemented with this structure, it is necessary to read the memristor state multiple times, greatly increasing the burden on the read circuit, and also limiting the slew rate. For example, to construct an 8-bit ADC, the output has 256 states, and 129 memristors are required to form a sequence. On average, 64 readings are required to find the memristor that is set to "on", and then the next memristor is judged. So whether the device is in the "on" state, the circuit has to be read 65 times to get the output state.
Too much time cost in the read operation limits the conversion speed of the ADC and there is much room for improvement.

**Improvement of ADC Design Based on Memristor**

In this paper, a new quantization circuit based on memristor is designed for ADCs, as shown in Figure 2, which is an upper triangular resistance matrix formed by memristors. The \( i \)-th row has \( i \) memristors, and the memristors in each row are connected in series. The lines are connected in parallel, the left terminal is connected to the input signal, and the right terminal is grounded.

Initially, all memristors are "on" states. The input terminal applies a pulse signal with a width of \( \Delta T \), where \( \Delta T \) is the minimum time for pulse changing the memristor’s state when the voltage \( V_{in} \) exceeds the switching threshold value \( V_{th} \). Since each memristor is in series relationship, the whole applied voltage is divided by each other, the voltage amplitude of each memristor in the \( i \)-th row is shrinked to \( V_{in}/i \). When \( V_{in} > i \cdot V_{th} \), each memristor of the row number less than \( i \) is switched from the "on" state to the "off" state, and the input pulse is quantized as \( iV_{th} \), and \( V_{th} \) is the minimum quantization unit.

![Figure 2. New design of Analog-to-Digital Converter Module Based on Memristor.](image)

Let’s take a 3-bit ADCs as an example to illustrate the design of this article. When the system has a input signal \( V_{in} \), which equals \( 2.3V_{th} \). Since \( 2.3V_{th} > 2V_{th} \), one memristor in the first row and two memristors in the second row are converted to the "off" state, and the memristors on the row from line 3 to line 7 remain "on". That is, the input is quantized to \( 2V_{th} \), and \( V_{th} \) is the quantized minimum unit \( \Delta V \). The high resistance state of the memristor indicates a logic value of ‘1’, and the low resistance state indicates a logic value of ‘0’. Finally, the quantization code stored in the memristors is 000011.

The quantization coding scheme is shown in the following table:

<table>
<thead>
<tr>
<th>The amplitude of input signal</th>
<th>The coding result</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 0 \leq V_{in} &lt; \Delta V )</td>
<td>0000000</td>
</tr>
<tr>
<td>( \Delta V \leq V_{in} &lt; 2\Delta V )</td>
<td>0000001</td>
</tr>
<tr>
<td>( 2\Delta V \leq V_{in} &lt; 3\Delta V )</td>
<td>0000011</td>
</tr>
<tr>
<td>( 3\Delta V \leq V_{in} &lt; 4\Delta V )</td>
<td>0000111</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>

Since the half of the converted memristor matrix is in the "on" state and the other half is in the "off" state, the order is arranged, so the strategy of folding the half can be used when reading the quantized result. Since the states of the individual memristors on each line are the same, each row only needs to read the state of one memristor. i.e. The \( n \)-bit ADCs module has a \((2^n-1)\) line, and first reads the state of the last memristor of the \(2^n-2\)-th row, if it is the "on" state, Then read the last line of the \((2^n-2, 2^n-1)\) line; if it is "off state, read the second \((2^n-2, 2^n-3)\) the state of the row. By analogy, until an \( i \)-th behavior is "off" and its neighboring behavior is "on", the quantized result can be judged as \( iV_{th} \). Theoretically, for an \( n \) bits quantized results, the averaged comparaison operation needs \( n+1 \) times.
Similarly, taking the above 3-bit ADC as an example again, when a signal $V_{in}$ having a size of $2.3V_{th}$ is input to the left end of the system, the step of reading the quantized state is further explained, which further explains the reading strategy. First read the last memristor on line 4 and find that its status is "on". Then read the last memristor on line 2 and find that its status is "off". Then read the last memristor on line 3 and find that its status is "on". Therefore, after three reading operations, it can be judged that the quantization result is $2V_{th}$.

### Simulation and Discussion

The software used in this simulation was OrCAD Capture CIS, using the Spice simulation tool. The 3-bit quantization circuit in Figure 2 was constructed using the threshold memristor model. In this model, the equation (1) and (2) would be rewritten as:

$$I_M = [M (x, V_M)]^{-1}V_M$$  \hspace{1cm} (3)  

$$\frac{dx}{dt} = \{\beta V_M + 0.5(\alpha - \beta)[|V_M + V_{th}| - |V_M - V_{th}|]\} [\theta(V_M)\theta(R_{OFF} - x) + \theta(-V_M)\theta(x - R_{ON})]$$  \hspace{1cm} (4)  

where $V_{th}$ is threshold voltage, $R_{OFF}$ and $R_{ON}$ are the high resistance and low resistance of memristor, respectively. $\alpha$ and $\beta$ are the fitting variable. Here the memristor simulation parameters are: $R_{ON}=1000$, $R_{OFF}=6K$ and the threshold voltage is $V_{set}$ to $0.1V$.

The simulation schematic is as follows:

Set the input signal to $3V_{th}$, and the output result is as shown in the figure below. The last memristor in the first, second, and third rows becomes high resistance, and the last memristor in the remaining rows is in a low resistance state. The simulation result is shown in Figure 3.

![Simulation Schematic](image)

Figure 3. a–g is the resistance of the last memristor in the 1st row to the 7th row when the voltage is $0.3V$.

Another test bench is to set the input signal $4.9V_{th}$. The last memristor on the 1st, 2nd, 3rd, and 4th lines should become high resistance, and the last memristor remains unchanged in 3 lines. The simulation result is shown in Figure 4.
In this paper, a new quantization circuit based on memristor is designed for ADCs. Compared with the existing memristor-based ADC design, the power consumption is lower, the circuit is easier to implement, and the conversion speed is faster.

**Summary**

In this paper, a new quantization circuit based on memristor is designed for ADCs. Compared with the existing memristor-based ADC design, the power consumption is lower, the circuit is easier to implement, and the conversion speed is faster.

**Acknowledgement**

This work was supported by the National Natural Science Foundation of China (No. 61471377, 61604177, 61704191 and 61701509).
References


