FIR Multiphase Decimation Filtering Method Based on Base 2 FFT

Te-liang WANG*, Jun-gang YANG and Yu MO

School of Electrical Science, National University of Defense Technology, Changsha 410073, China

Corresponding author

Keywords: Data compression, Base 2 FFT, FIR, Multiphase decimation filter.

Abstract. It is very important to improve the data throughput of decimation filter for radar systems with large amount of data and high requirement of real-time imaging. On the basis of the analysis of the traditional Finite Impulse Response (FIR) multiphase decimation filtering method, combined with Field Programmable Gate Array (FPGA), we put forward FIR multiphase decimation filtering method based on base 2 Fast Fourier Transform (FFT). In this paper, the mathematical model of base 2 FFT for FIR multiphase decimation filter is studied, and the hardware structure of multiphase decimation filtering method based on base 2 FFT is presented. The simulation results show that the proposed method can effectively preprocess the echo data of radar system and improve the real-time performance.

Introduction

According to Nyquist theorem, the sample rate of a discrete-time signal must be greater than or equal to twice its bandwidth, otherwise further reducing the sample rate will cause the spectrum aliasing. Therefore, we usually use a low-pass filter to reduce the signal bandwidth before reducing the signal sample rate. As shown in Fig. 1 is a typical structure of decimation filter, composed of a low-pass filter and a sampler. The operating mode is to filter the data first and then sample it.

![Figure 1. Typical structure of decimation filter.](image)

The basic of typical decimation filter is simple, but when the signal has the characteristic of high frequency, the low pass filter needs to deal with a large amount of data. Also, most of the data, processed by a low-pass filter, will be abandoned after being sampled. This is not only a great pressure to hardware implementation but also a waste of hardware resources. Therefore, if we can sample the signal first and then filter it, we can save the hardware resources, reduce the calculation amount and increase operation velocity.

To sample the data first and then filter it, we have to devise the parallel processing structure of FIR at first. The common algorithms to realize the parallel processing structure of FIR include Iterated Short Convolution Algorithm (ISCA) [1,2], Fast FIR Algorithm (FFA) [3] and improved algorithms based on FFA [4-9]. In addition, Sinha P et al. designed a digital signal processing basic unit to construct parallel FIR filter [10], and Conway et al. implemented the parallel FIR filter by using the theory of number theoretic transform [11]. These methods are low-complexity and easy to realize, but do not give full play to the advantages of abundant hardware resources of the 7th generation FPGA released by Xilinx in 2012. And in recent years, with the application of radar systems to security check and other fields, the requirement of real-time data processing is getting higher. Therefore, it is necessary to study a FIR multiphase decimation filtering method with high real-time performance.

Based on the research and analysis of basics of the traditional FIR multiphase decimation filtering method, this paper studied the mathematical model of base 2 FFT algorithm for FIR multiphase decimation filter, and proposed a FIR multiphase decimation filtering method based on base 2 FFT algorithm and its hardware implementation structure.
Basics of Traditional FIR Multiphase Decimation Filter

For the sequence \( x(n) \) with \( N \) points, the order of the FIR filter is \( N - 1 \), and its FIR filter output can be expressed in \( Z \) domain as

\[
Y(z) = X(z)H(z) = \sum_{n=0}^{N-1} x(n)z^{-n} \sum_{n=0}^{N-1} h(n)z^{-n} \tag{1}
\]

If the decimation factor is \( K \), then \( K \)-phase decomposition can be applied to \( X(z) \) and \( H(z) \).

\[
X(z) = x(0) + x(1)z^{-1} + \ldots + x(N-1)z^{-(N-1)}
= \left(x(0) + x(K)z^{-K} + \ldots + x(Kl)z^{-Kl}\right)
+ \left(x(1)z^{-1} + x(1+K)z^{-(1+K)} + \ldots + x(1+Kl)z^{-(1+Kl)}\right)
+ \ldots
+ \left(x(K-1)z^{-(K-1)} + x(K-1+K)z^{-(K-1+K)} + \ldots + x(K-1+Kl)z^{-(K-1+Kl)}\right)
= \left(x(0) + x(K)z^{-K} + \ldots + x(Kl)z^{-Kl}\right)
+ \left(x(1) + x(1+K)z^{-K} + \ldots + x(1+Kl)z^{-Kl}\right)z^{-1}
+ \ldots
+ \left(x(K-1) + x(K-1+K)z^{-(K-1)} + \ldots + x(K-1+Kl)z^{-(K-1)}\right)z^{-(K-1)}
= X_0\left(z^K\right) + z^{-1}X_1\left(z^K\right) + \ldots + z^{-(K-1)}X_{K-1}\left(z^K\right)
= X_0 + z^{-1}X_1 + \ldots + z^{-(K-1)}X_{K-1} \tag{2}
\]

\[
H(z) = H_0 + z^{-1}H_1 + \ldots + z^{-(K-1)}H_{K-1} \tag{3}
\]

Where \( K \leq N \), and \( N \) can be divisible by \( K \), i.e. \( \frac{N}{K} = l \). If \( N \) can’t be divisible by \( K \), then we can remove the excess items in the Eq. 2 and Eq. 3. Substituting Eq. 2 and Eq. 3, we can write Eq. 1 as,

\[
Y(z) = \left(H_0X_0 + z^{-K}H_{K-1}X_1 + \ldots + z^{-K}H_1X_{K-1}\right)
+ \left(H_1X_0 + H_0X_1 + z^{-K}H_{K-1}X_2 + \ldots + z^{-K}H_1X_{K-1}\right)z^{-1}
+ \ldots
+ \left(H_{K-1}X_0 + H_{K-2}X_1 + \ldots + H_0X_{K-1}\right)z^{-(K-1)}
= Y_0\left(z^K\right) + Y_1\left(z^K\right)z^{-1} + \ldots + Y_{K-1}\left(z^K\right)z^{-(K-1)}
= Y_0 + z^{-1}Y_1 + \ldots + z^{-(K-1)}Y_{K-1} \tag{4}
\]

The matrix form of Eq. 4 is as following equation

\[
\begin{bmatrix}
Y_0 \\
Y_1 \\
\vdots \\
Y_{K-1}
\end{bmatrix}
= \begin{bmatrix}
H_0 & z^{-K}H_{K-1} & \ldots & z^{-K}H_1 \\
H_1 & H_0 & \ddots & z^{-K}H_2 \\
\vdots & \vdots & \ddots & \vdots \\
H_{K-1} & H_{K-2} & \ldots & H_0
\end{bmatrix}
\begin{bmatrix}
X_0 \\
X_1 \\
\vdots \\
X_{K-1}
\end{bmatrix} \tag{5}
\]
Since the decimation factor is $K$, for every $K$ output data of the filter, we only use one of the data, and the other $K-1$ data are discarded. Eq. 5 can be composed as

$$
[Y_{K-1}] = [H_{K-1} \ H_{K-2} \ \cdots \ H_0] \begin{bmatrix} X_0 \\ X_1 \\ \vdots \\ X_{K-1} \end{bmatrix}
$$

(6)

Comparing Eq. 5 with Eq. 6, the method which we sample the signal first and then filter it by FIR multiphase decimation filter can reduce the calculation amount to $\frac{1}{K}$ of the original with the typical method.

**FIR Multiphase Decimation Filtering method Based on Base 2 FFT**

**The Design Idea**

The FIR filter output of input data $x(n)$, in frequency domain, is given by the following equation:

$$
Y(k) = \sum_{n=0}^{N-1} x(n) W_N^m h(n) W_N^k = X(k)H(k)
$$

(7)

By the means of zero padding to sequence $x(n)$ with $N$ points, we can make $N = 2^M$. According to the basics of the base 2 FFT algorithm, the operation flow diagram of the base 2DIT-FFT algorithm is shown in Fig. 2.

**Figure 2.** The operation flow diagram of the base 2 DIT-FFT algorithm.

$W_N^k$ is a rotation factor. As shown in Fig. 2, the base 2 DIT-FFT algorithm has the following characteristics: The order of input sequence $x(n)$ and output sequence $X(k)$ is followed by the principle of reversing bit code. The sequence with $N$ points while $N = 2^M$ can be divided into $M$ stages. And there are $\frac{N}{2}$ butterfly processing elements at each stage. Each butterfly operation consists of one complex multiplication, one complex addition and one complex subtraction. The interval between two data points of the same butterfly operation in stage $m$ is $2^{m-1}$, and there are
\(2^{m-1}\) different expressions of rotation factor in stage \(m\), where \(m = 1, 2 \ldots M\). When the algorithm is implemented in hardware, the input data and output data of the same butterfly processing element can share the memory cell.

Therefore, we can transform the input data of the filter into frequency domain by using the base 2 DIT-FFT, and remove the invalid operations of the base 2 FFT to complete the decimation of the input data. Then we can complete the FIR filtering of the base 2 FFT output data in frequency domain to realize the FIR multiphase decimation filtering.

**The Mathematical Model**

Based on the above studies, we need to develop a mathematical model that we can remove the invalid operations of the base 2 FFT algorithm. We simplified the operation flow diagram of the base 2DIT-FFT algorithm in Fig. 2 as shown in Fig. 3.

\[
\begin{align*}
X(0) & \quad X_1(0) \quad X_2(0) \quad \ldots \quad X_{m-1}(0) \quad X_m(0) \\
X(2^m-1) & \quad X_1(1) \quad X_2(1) \quad \ldots \quad X_{m-1}(1) \quad X_m(1) \\
\vdots & \quad \vdots \quad \vdots \quad \ddots \quad \vdots \quad \vdots \\
X(N-1) & \quad X_{N-2}(N-1) \quad X_{N-3}(N-1) \quad \ldots \quad X_{N-2}(N-1) \quad X_{N-3}(N-1)
\end{align*}
\]

Figure 3. The simplified operation flow diagram of the base 2 DIT-FFT algorithm.

As we all know, the interval between two data points of the same butterfly operation in stage \(m\) is \(2^{m-1}\). After further analysis and induction, we can see that if one of the output data of a butterfly processing element is \(X_m(n)\), then the other one is shown as

\[
\begin{cases}
X_m(n+2^{m-1}), & \text{when } \frac{n-1}{2^{m-1}}-(n-1) \mod 2^{m-1} \text{ is an even number} \\
X_m(n-2^{m-1}), & \text{when } \frac{n-1}{2^{m-1}}-(n-1) \mod 2^{m-1} \text{ is an odd number}
\end{cases}
\]  

(8)

**The Hardware Structure**

There are 480,000 logical units in the Kintex-7 FPGA which is cost effective. Considering the total requirements of hardware resources for a radar system, we can guarantee the implementation of at least 8,000 butterfly processing elements on the Kintex-7 FPGA.

Therefore, if the required amount of butterfly operations was less than 8000, we can use array processing structure of hardware, as shown in Fig. 4, to realize FIR multiphase decimation filtering.
The ROM stores the frequency response functions \( H(k) \) of the filter and the rotation factors \( W_N^k \). BPE refers to butterfly processing element. MUP refers to multiplier. And \( b(m) \) refers to the number of butterfly processing elements at stage \( m \). In array processing structure of hardware, all the operations are processed in parallel.

If the required amount of butterfly operations was more than 8000, we can use parallel iteration processing structure of hardware, as shown in Fig. 5, to realize FIR multiphase decimation filtering.

In parallel iteration processing structure of hardware, the butterfly operations of the same stage are processed in parallel, and the stages are processed in sequence.

**Simulation Experiment and Performance Analysis**

**Simulation Experiment**

The method of this paper is simulated by MATLAB, and the simulation parameters are listed in Table 1.

<table>
<thead>
<tr>
<th>Signal Type</th>
<th>Noise Type</th>
<th>Center Frequency</th>
<th>Sampling Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Complex exponential signals</td>
<td>White noise</td>
<td>21 [MHz]</td>
<td>81 [MHz]</td>
</tr>
<tr>
<td>Number of Data</td>
<td>Data-width</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1024</td>
<td>16 [bit]</td>
<td>2</td>
<td>Ideal band-pass filter</td>
</tr>
</tbody>
</table>
Fig. 6 consists the theoretical modulus of the amplitude-frequency response of the simulation data. Fig. 7 has the modulus of the amplitude-frequency response of the FIR decimation filter output data. And the modulus of the amplitude-frequency response of the output data of the FIR multiphase decimation filter based on base 2 FFT are shown in Fig. 8.

Figure 6. Modulus of the amplitude-frequency response of the simulation data.

Figure 7. Modulus of the amplitude-frequency response of the FIR decimation filter output data.

Figure 8. Modulus of the amplitude-frequency response of the filter output based on proposed method.
Comparing the simulation results in Fig. 6, Fig. 7 and Fig. 8, we proved that the FIR multiphase decimation filtering method proposed in this paper can effectively process radar echo data.

**Performance Analysis**

Suppose the time for a butterfly operation is $T$, the time for a multiplication is $t$, the number of tap-weight is $N$ and $N = 2^M$.

All the operations of array processing structure of hardware are processed in parallel and $T > t$, so the time for the FIR multiphase decimation filtering of $N$ data is $T$ in theory. In parallel iteration processing structure, the butterfly operations of the same stage are processed in parallel, and the stages are processed in sequence, so the time for the FIR multiphase decimation filtering of $N$ data is $M \cdot T + t$.

**Conclusion**

This paper analyzed the basics of traditional FIR multiphase decimation filter, and put forward the mathematical model of base 2 FFT algorithm applied to FIR multiphase decimation filter. Then we used the principle of multiphase decimation filter to simplify the operation process of the base 2 FFT. Thus we can convert data into frequency domain by the simplified base 2 FFT algorithm to realize the FIR multiphase decimation filter. And we put forward two structures of the hardware implementation of the method. This method is an efficient parallel processing operation, which can make a good use of all the available hardware resources and the parallel processing advantage of FPGA, and can greatly improve the operation speed of FIR decimation filtering.

**References**


