A 2.14GHz Driver-stage Power Amplifier for Doherty Power Amplifier

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ABSTRACT

This paper presented a high power amplifier drive a Doherty power amplifier. By using computer software to design and test instrument to adjust, the result shows the driver-stage power amplifier that is made of the MRF8S21100H from NXP company meet the 15dB gain, and 42% power added-efficiency (PAE) at the maximum output power. Comparing with the traditional design method, this method has the advanced success rate and design cycle.

KEYWORDS

Power Amplifier, Driver-stage, and High Power.

INTRODUCTION

The radio frequency power amplifier (RFPA) is a key component of the wireless transmitter, its power output, efficiency and linearity affects the whole performance of the communication system directly [1]. Sometimes, a single-stage power amplifier cannot provide the required power signal. Therefore, a driver-stage power amplifier is proposed. The driver-stage power amplifier [2, 3] can provide sufficient input power signal for the final-stage power amplifier. In addition, the Doherty power amplifier [4, 5] has been studied vigorously. The Doherty power amplifier can maintain high efficiency at high output power. Most of the signal source cannot provide sufficient power signal for the Doherty power amplifier. Hence, the driver-stage power amplifier determines whether the Doherty power amplifier can work well under this circumstance. In certain cases, numerous power amplifiers will be composed to the multilevel system to provide sufficient power signal for the communication system.

The traditional design method is the power amplifier circuit design on printed circuit board (PCB). This approach requires RF engineers with considerable experience. In addition, debugging the circuit most of the time is rather time-consuming. In this paper, we proposed a design method of a driver-stage power amplifier for a Doherty power amplifier working at 2.14 GHz. The simulation and optimization are accomplished by Advanced Design System (ADS), and PCB debugging can return the design suggestion to ADS. According to the design and measurement, this method can lower the cost, reduce the difficulty, and shorten the cycle of the design.

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A. Select of power amplifier

We choose AB-class power amplifier to design this driver-stage power amplifier. Typical AB-class power amplifier has a conduction angles which is lesser than 360°, but greater than 180°. As the conduction angle reduces, the DC component drops but the fundamental RF component remains very nearly constant [6].

Then, we select MRF8S21100H from NXP Company to accomplish entire design and debugging. MRF8S21100H is designed for 2110 to 2170 MHz, this LDMOS can be used in AB-class and C-class for all typical cellular base station modulation formats.

B. Output and input match network design

The output match network and input match network determines the power amplifier performance directly. We design the output match network at first. The ADS has load-pull and source-pull system, which can measure the optimum load impedance and source impedance from MRF8S21100H model.

By using load-pull system [7, 8, and 9], the power circle and the efficiency circle can be found in Smith chart. The optimum impedance is the central point in the circle. The result of load-pull system shows that the optimum load impedance is (6.1-j*2.3) Ohm.

Then, inserting a linear type of match network between transistor and output port to ensure signal can be transmitted with low loss. In addition, we need a drain bias circuit to supply drain voltage. The final output match network is shown in Figure.1.

![Figure 1. Result of the load-pull.](image1)

![Figure 2. The model of output match network.](image2)
The process of input match network design is consistent with output match network design. After using source-pull system, the optimum source impedance is defined as (6.7-j*7.3) Ohm. We also design a linear type match network between input port and gate. The same as output match design, a gate supply voltage circuit is needed. However, the wide of the micro strip line in gate voltage supply circuit is thinner than drain voltage supply circuit. Because the drain voltage supply circuit needs maintain the hundreds of milliamps current, but gate voltage supply circuit only maintain a very small current.

Combined with the input match, output match and MRF8S21100H we can acquire an intact power amplifier from the ADS.

C. Overall circuit simulation

To obtain the performance of designed power amplifier, the ADS schematic simulation is acquired. The schematic diagram of the driver-stage power amplifier circuit is shown in Figure 3. In this design, the drain voltage is 28V, and the current is 500mA.

As shown in Figure 4, the gain of power amplifier is 15.5dB, the largest output power is 46dBm, and the PAE at the maximum output power is 58%.

As usual, EM model simulation is necessary to ensure the rationality of circuit after the schematic simulation. During the EM model simulation, it is found that the performance does not have any deterioration. Therefore, the material printed circuit board (PCB) can be made after the design by ADS.
TESTING OF THE DRIVER-STAGE POWER AMPLIFIER

By using the layout assistant in the ADS, circuit model can be exported as layout file. We can open and amend this layout file by the Computer Aided Design (CAD). And an aluminum plate is the same size as the PCB is reacquired to connect the MRF8S21100H as a cooling pin.

The material of PCB Rogers 4350 is selected to make this circuit. The Rogers 4350 is the high frequency circuit material, and it is glass reinforced ceramic laminate designed for performance sensitive, high volume commercial applications. We can use this circuit material to ensure the performance.

After debugging, an extra micro strip is added to acquire the better performance. Then, we need to measure the overall circuit performance. There are two processes during the entire measurement. The first step is to acquire the small signal performance, the data of S11 is essential. The performance of S11 influences the efficiency, the gain, the heat dissipation and more. The second step is the measurement of efficiency and gain. This process is a core process, the measurement is to test the power amplifier’s performance, and it is a step to verify the correction of the software design above. So this step is the most important step on the PCB measurement. The S11 from the measurement is shown in Figure.6.

![Figure 5. Layout and photograph of the driver-stage power amplifier.](image)

![Figure 6. The S11 curve of measurement.](image)
Figure 7. The performance of simulation and measurement.
It is found that the S11 is lower than -16dB, which means we can ensure almost all of the input signal reach the MRF8S21100H’s gate through input match network. And such S11 can ensure the transistor have normal performance when working at big signal.

As shown in Figure.7, when the power amplifier works at 2140MHz, drain voltage is 28V and the current is 500mA, the gain is about 15dB, the largest output power is about 47dBm, and the PAE at the largest output power is about 41%. By contrast with the performance from software design, it is obviously that the performances from big signal measurement have a little degraded. The deterioration is inevitable. Because the computer design and simulation is under the ideal situation, computer cannot think about the complex actual circumstances. But the overall measurements are under the real condition, there are so many potential factors impact the performance of the power amplifier, such as the circuit machining precision, sample transistor condition. After all, the performance of power amplifier has some deterioration, but it is acceptable.

CONCLUSION

In this paper, a driver-stage power amplifier for a Doherty power amplifier that worked at 2140MHz is proposed. After the processes of the design, simulation, debugging and measurement, the power amplifier can meet the prospective performance. All of the processes have been given in detail. The driver-stage power amplifier design method in this paper is more advanced than the traditional method. By using software design and PCB measurement which can make the overall design course more precise and fast. More than that, the power amplifier designed by using software can reduce the difficulty and the cost. In conclusion, this design processes can be a good way to design a power amplifier.

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REFERENCES

